

MODEL NAME : BAP10(15")/BAP20(17")  
PROJECT CODE : ANRBAP1000/ANRBAP2000  
PCB NO :  
DAC00004000 LA-D751P M/B(NV)  
DAC00005000 LA-D751P M/B(NV\_G3)  
DA4002AV000 LS-D751P LOGO\_15/B  
DA80017I000 LS-D752P LOGO\_17/B  
DA4002B000S LS-D753P PWR\_15/B  
DA4002AW000 LS-D754P PWR\_17/B  
DA80017J000 LS-D755P IO\_12L/B  
DA4002AY000 LS-D757P TRON\_LCD\_15/B  
DA4002AZ000 LS-D758P TRON\_REAR\_15/B  
DA80017K000 LS-D759P IO\_14L/B  
DA4002D4000 LS-D75AP TRON\_LCD\_17/B  
DA4002D5000 LS-D75BP TRON\_REAR\_17/B  
DA4002D7000 LS-D75CP TRON\_FRONT\_15/B  
DA4002D8000 LS-D75DP TRON\_FRONT\_17/B  
DA30000W300 LF-D751P Head\_15/B  
DA30000W400 LF-D752P Head\_17/B  
DA30000W401 LF-D752P Head\_17/B(For LOGO\_15/B)  
DA30000SY00 LF-D753P TRON\_15/B  
DA30000WX00 LF-D754P TRON\_17/B

ZZZ PCB@  
PCB 1JM LA-D751P REV0 M/B NV 16  
DAC00004000

ZZZ PCBG3@  
PCB 1JM LA-D753P REV0 M/B NV G3 16  
DAC00005000

ZZZ PCBR1@  
PCB 1FU LA-C901P REV1 M/B MLK 3  
DAC00004010


ZZZ PCBR3@  
PCB 1FU LA-C901P REV1 M/B MLK TRIP 3 A31!  
DAC00004011

ZZZ DAZR1@  
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02  
DAZ1FU00100

ZZZ DAZR3@  
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02 TRIPOD A31 !  
DAZ1FU00101

HDMI@ ROYALTY HDMI W/LOGO	
Part Number	Description
RO00000002RM	HDMI W/Logo:RO0000002RM

Layout Dell logo



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REV: X00  
PWB: XXXXX  
DATE: 1450-06

BAP20 NVG3 Skylake/Kabylake-H 45W

Skylake/Kabylake PCH with nVidia N17E-G3

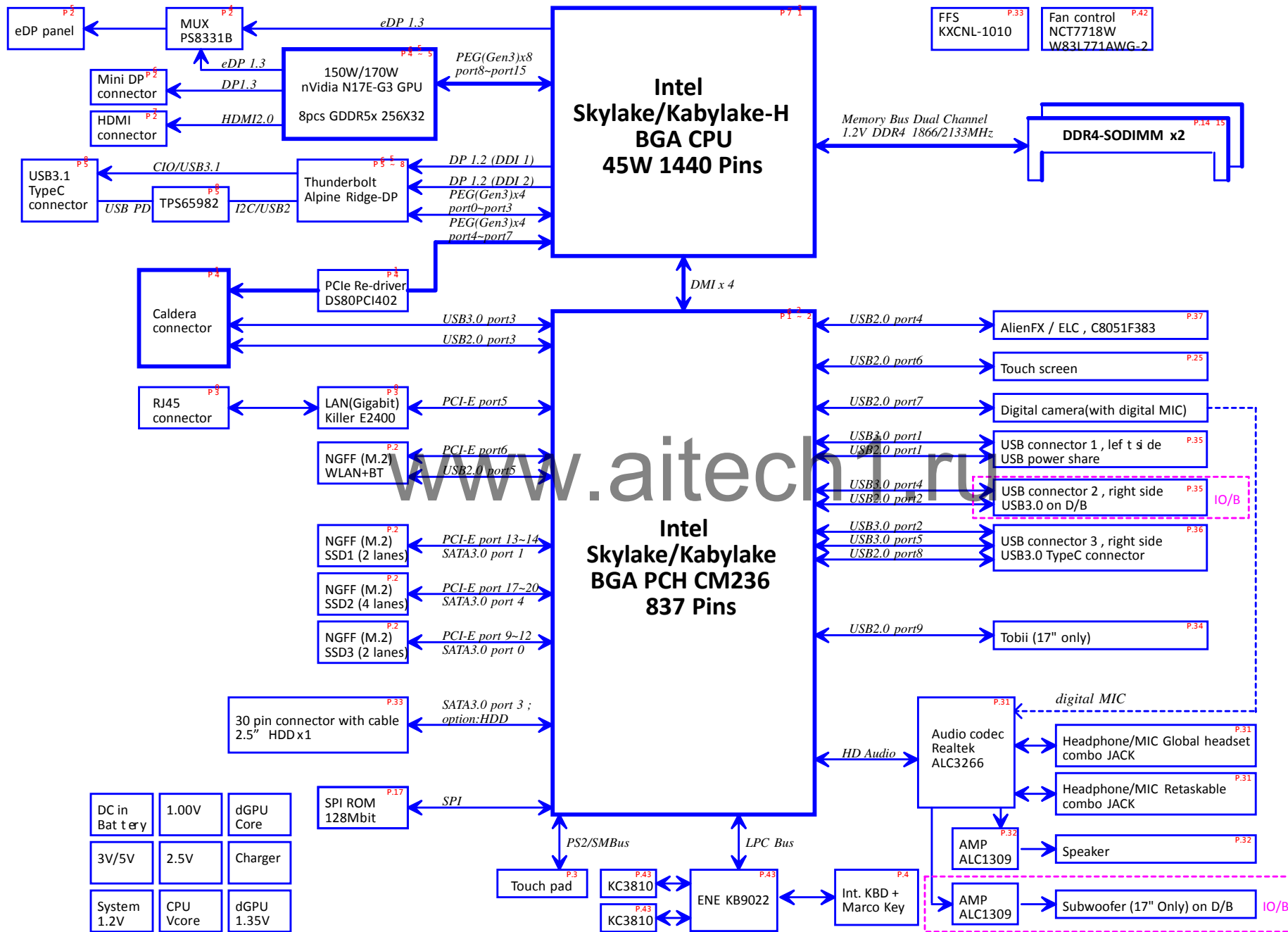
REV : 0.2 (X01)

2016.06.24

@ : Nopop Component  
EMI@,ESD@,RF@ : EMI/ESD/RF part

CONN@ : Connector Component  
@EMI@,@ESD@,@RF@ : Total debug Component

### Block Diagram

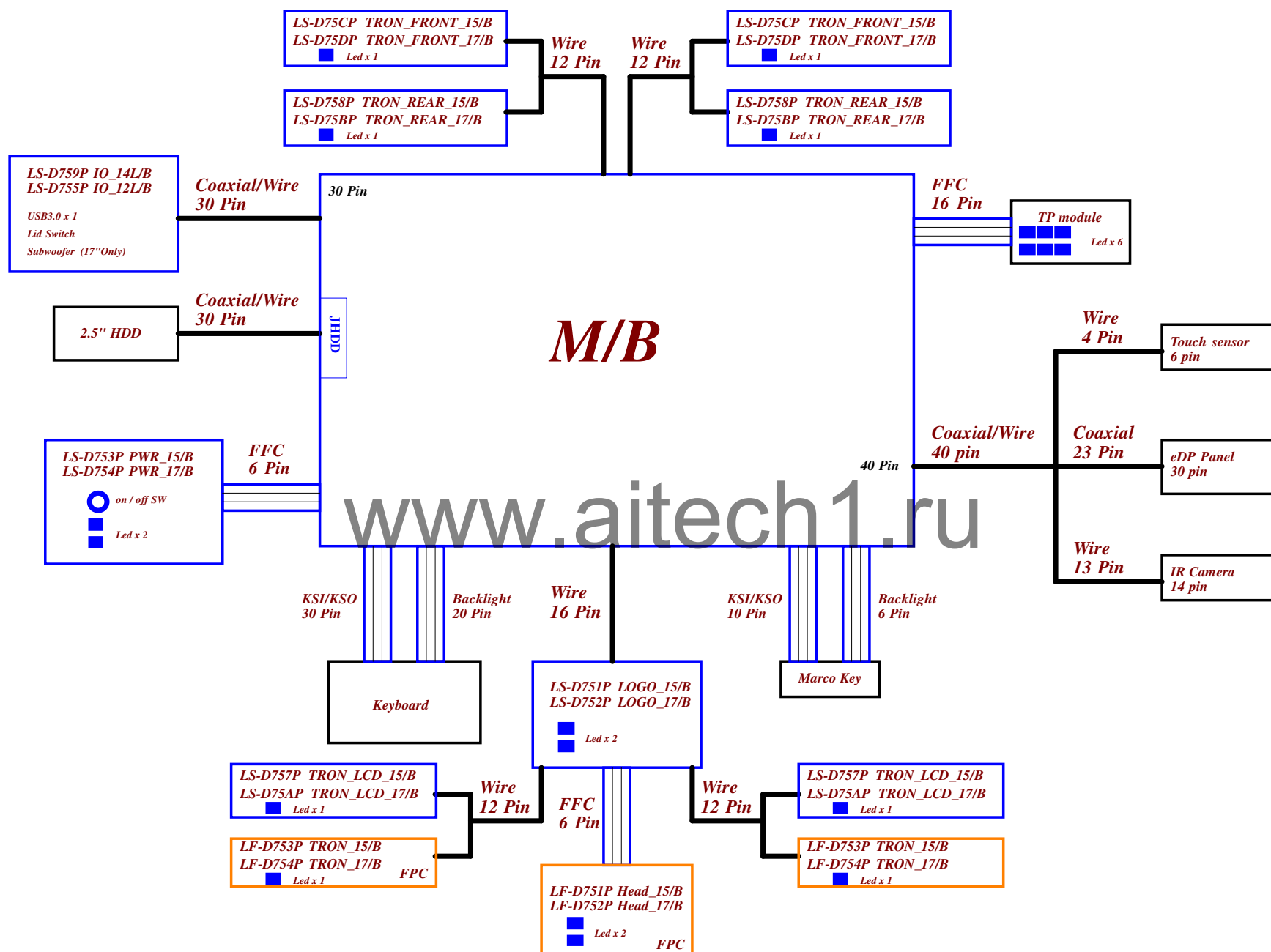


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PCB

FPC

Module



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						Size		Document Number		Rev	
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	+1.8VS power rail for GPU	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID TABLE

ID	PCB Revision
NV	AMD
0	10
1	11
2	12
3	13
4	14
5	15

PCH-H CM236

HSIO	USB3	PCIe	SATA3	Function
1	1			JUSB1,type A
2	2			JUSBC2,type C
3	3			Caldera
4	4			JIO,IO/B
5	5			JUSBC2,type C
6	6			
7	7	1		
8	8	2		
9	9	3		
10	10	4		
11		5		LAN
12		6		WLAN
13		7		
14		8		
15		9	0	JSSD3 M.2 2280
16		10	1	SATA
17		11		PCIe x4(When SSD/B exist)
18		12		
22		16	3	JSSD5/HDD SATA
21		15	2	JSSD4 SATA
20		14	1	JSSD1 SATA/PCIe x2
19		13	0	
23		17	4	
24		18	5	JSSD2 M.2 2280
25		19		SATA
26		20		PCIe x4

\* PCIe 13~16 in "Lane Reversal Mode". (HSIO Port 19~22)

USB2	Function
1	JUSB1(Powershare)
2	JIO(IO/B)
3	Caldera
4	ELC
5	Bluetooth
6	Touch screen
7	Camera
8	JUSBC2
9	Tobii
10	
11	
12	
13	
14	

Symbol Note :



Digital Ground



Analog Ground

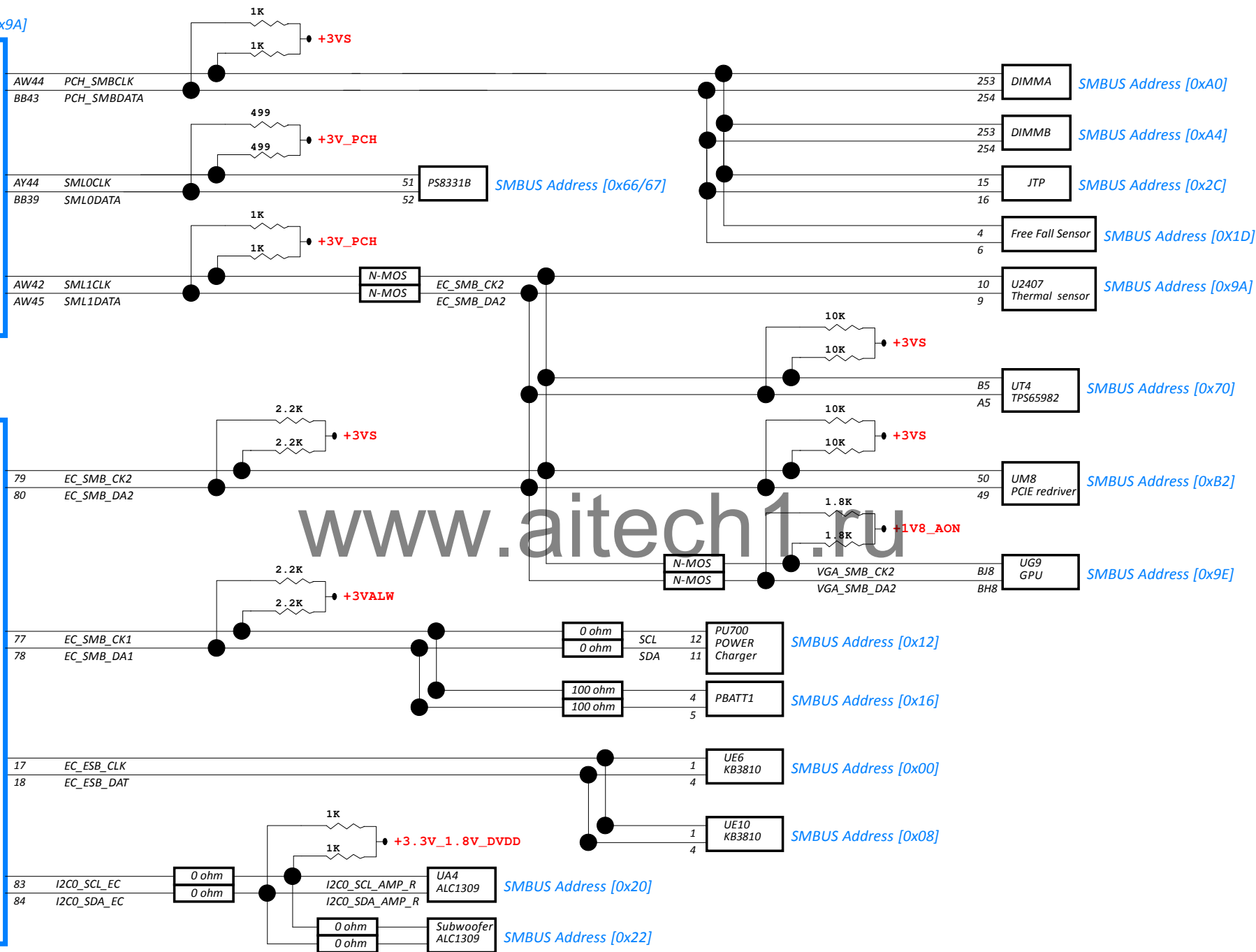
CPU,C  
DDR,D  
GPU,DP,HDMI,EDP,V  
LAN,L  
AUDIO,A  
NGFF,N  
USB,U  
CALDERA,M  
HDD,S  
ELC,E  
FAN,F  
TP,T  
KBC,K  
DC,O



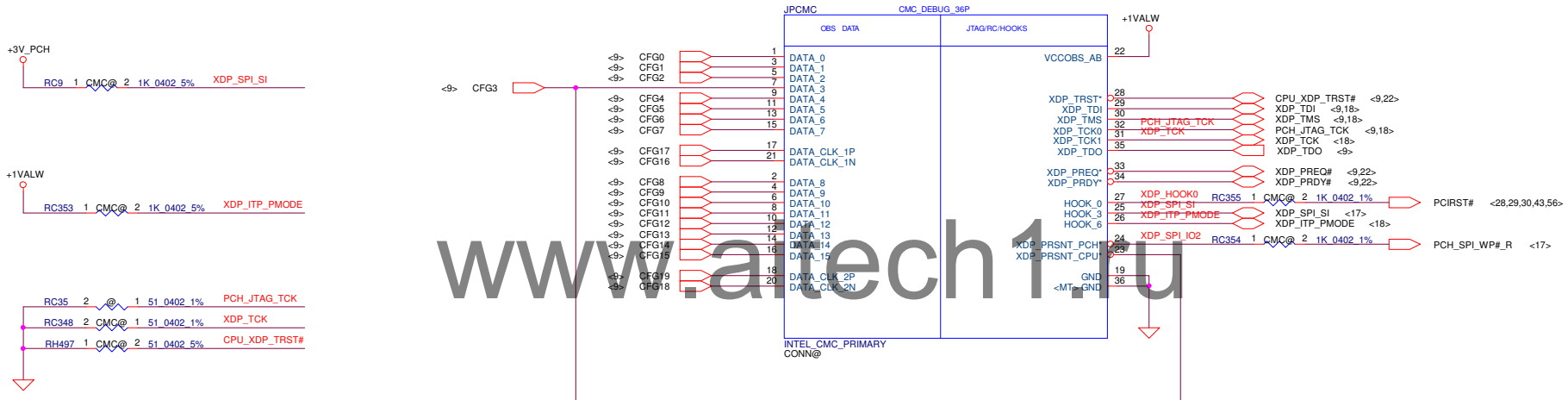
SMBUS Address [0x9A]

Kaby Lake  
PCH-H

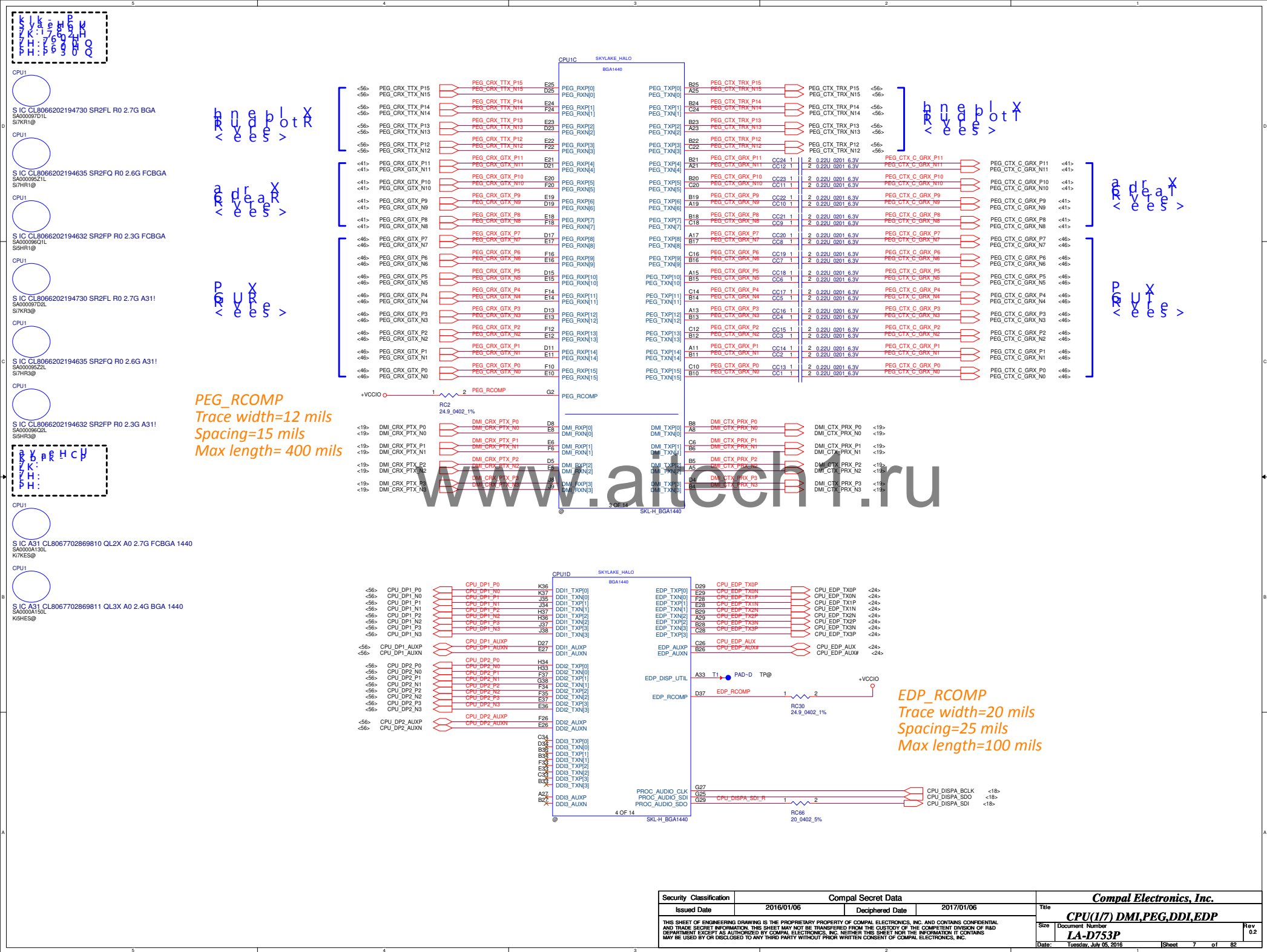
KBC  
KB9022QD



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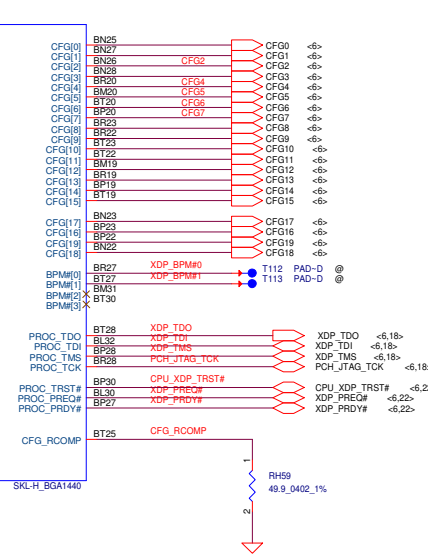


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										Size Document Number	
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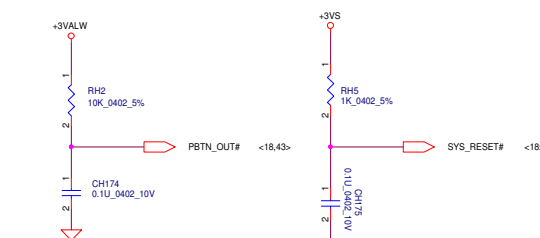
CFG2 1 RH184 2 1K\_0402\_5%

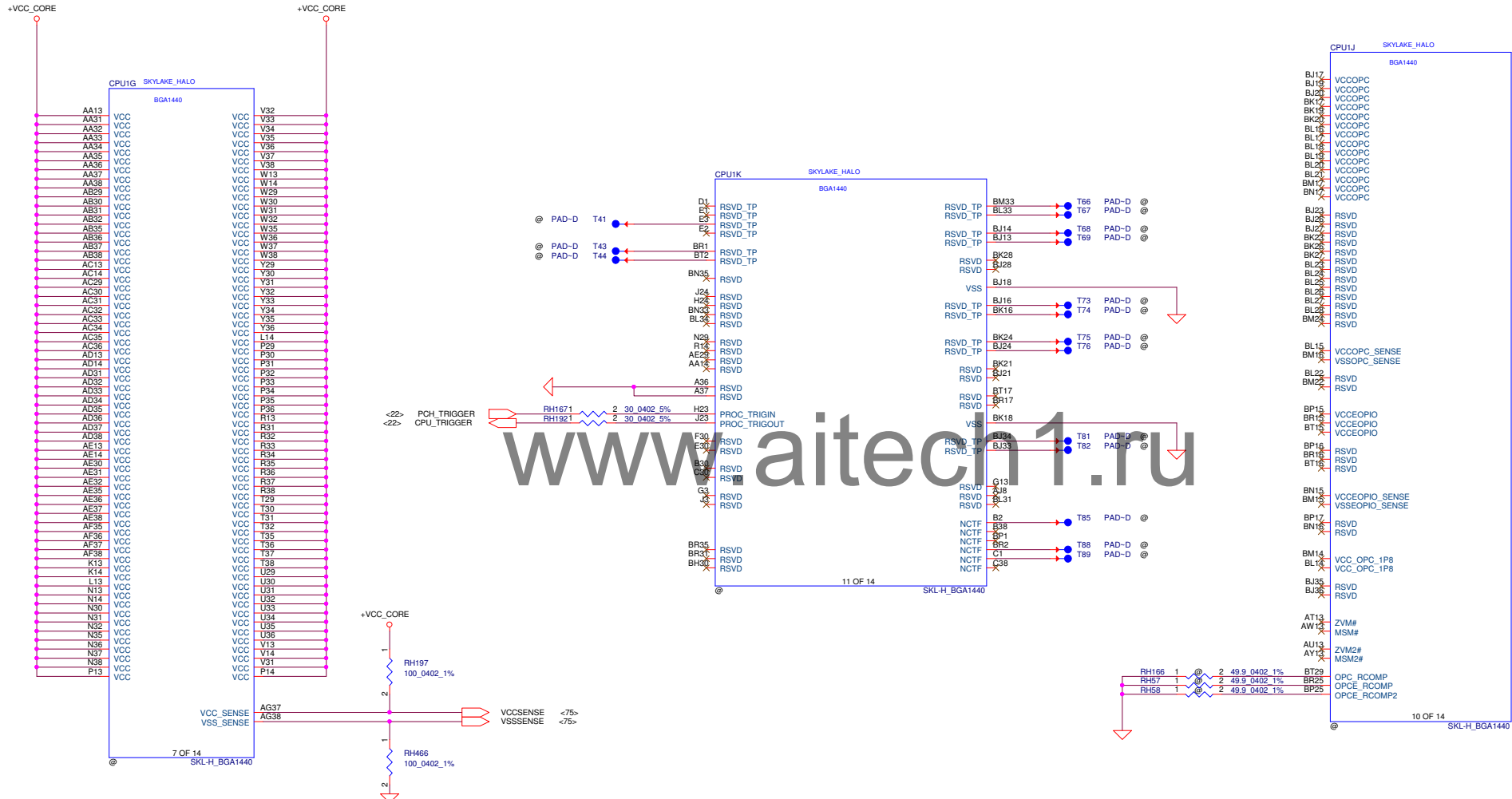
CFG4 1 RH185 2 1K\_0402\_5%

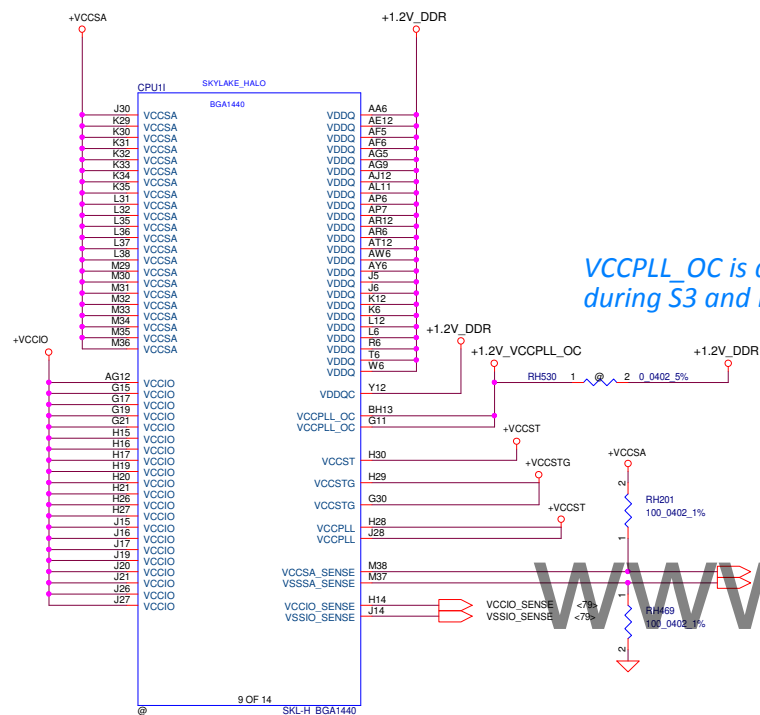
CFG5 1 2  
RH186 1K\_0402\_5%

CFG6 1 2  
RH187 1K\_0402\_5%

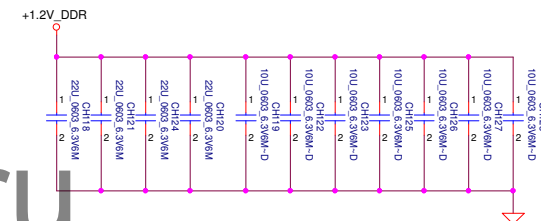
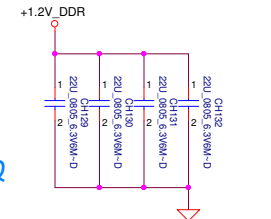
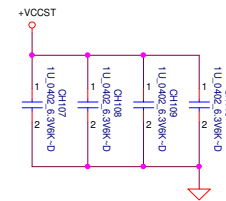
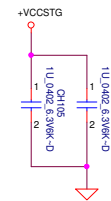
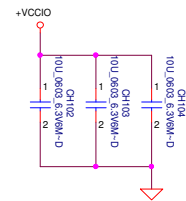
CFG7 1 2  
RH188 1K\_0402\_5%





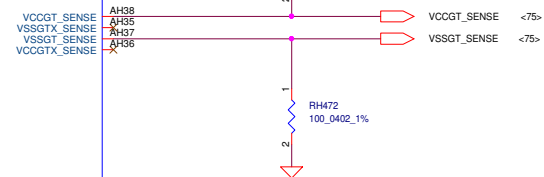
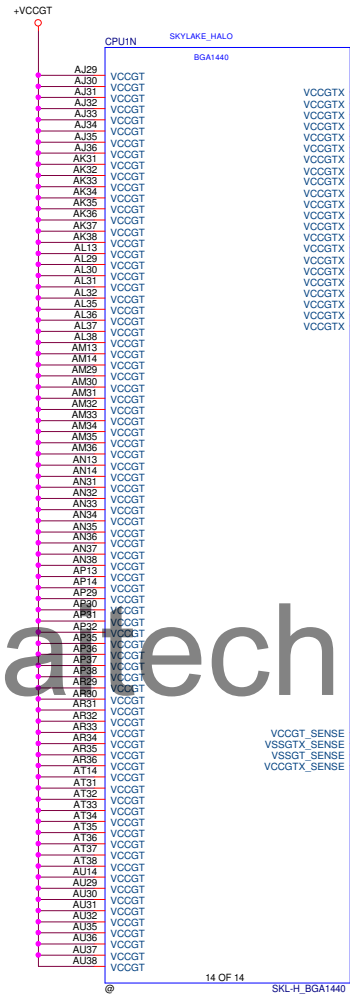
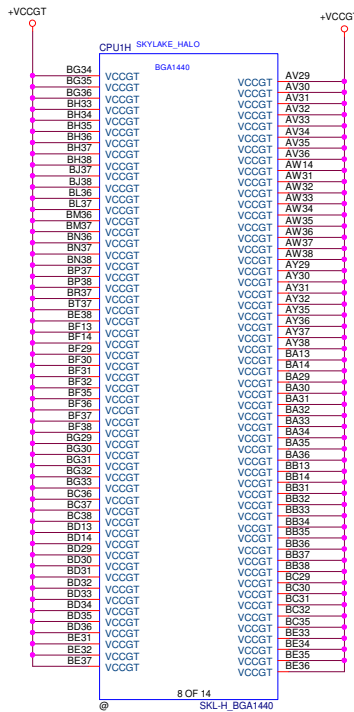


*VCCPLL\_OC is allowed to be turned of  
during S3 and DS3 if it is not powered directly from VDDQ*



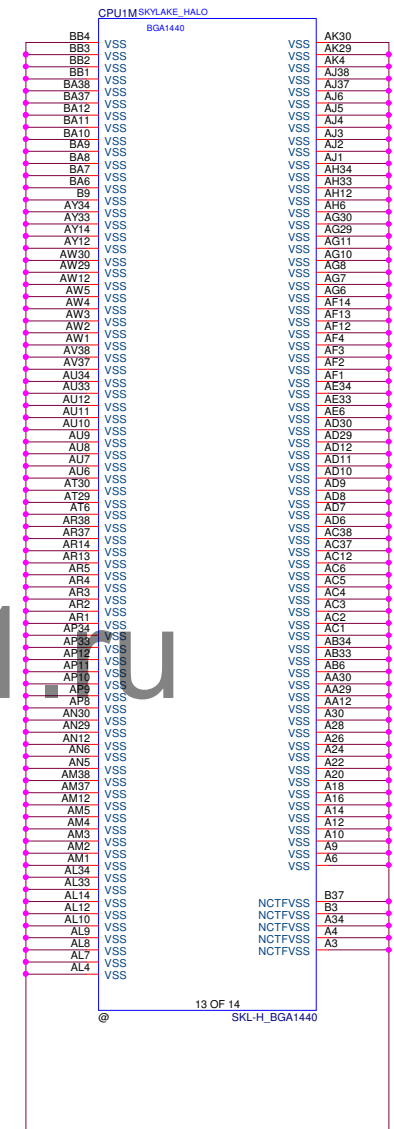
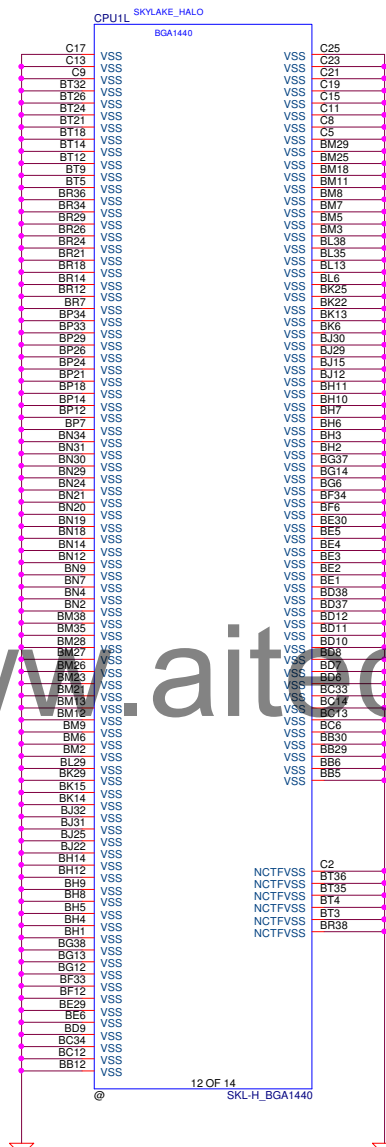
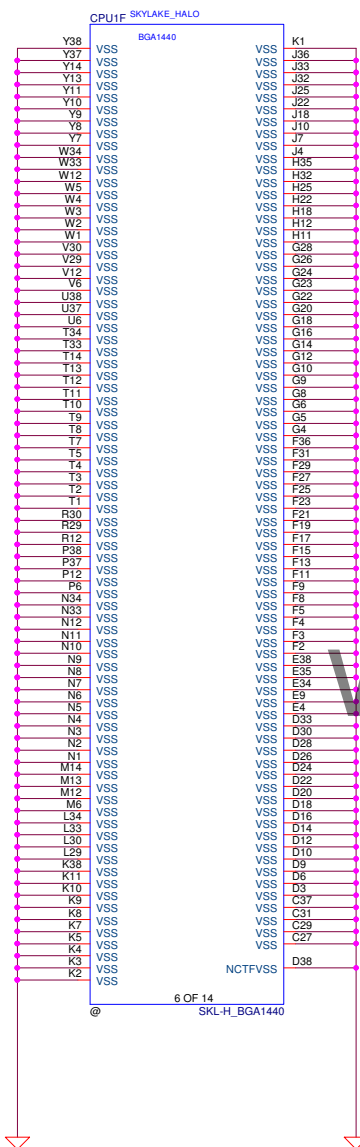
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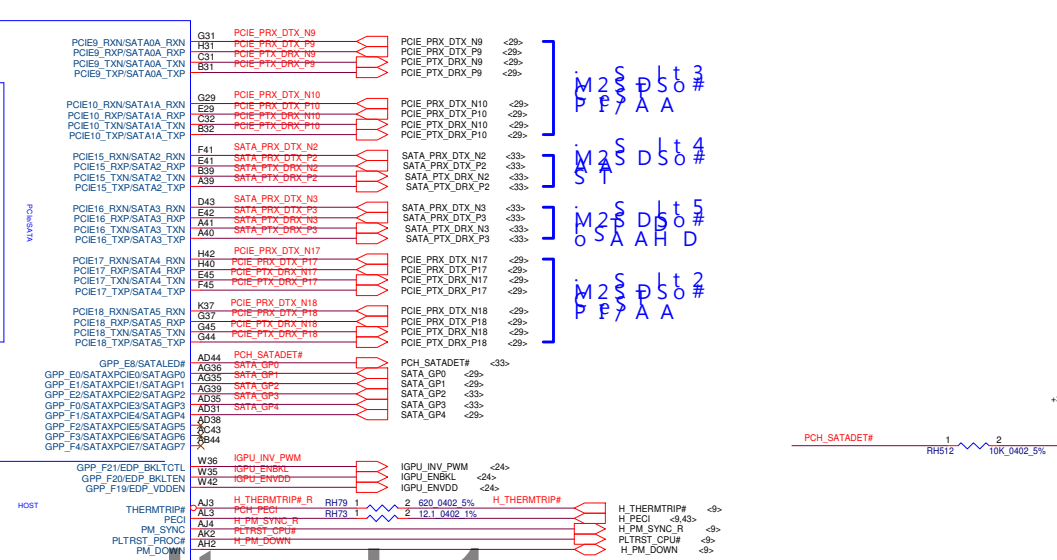


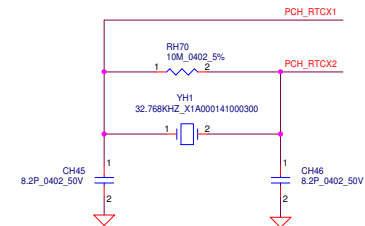


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The schematic diagram illustrates the XTAL24 circuit. It features a 24MHz crystal (YH2) connected to a 1M 0.002 5%-D resistor (RH72). The circuit is powered by a 15P\_0402\_50V capacitor (CH47) and a 15P\_0402\_50V capacitor (CH48). The XTAL24\_IN and XTAL24\_OUT pins are shown.

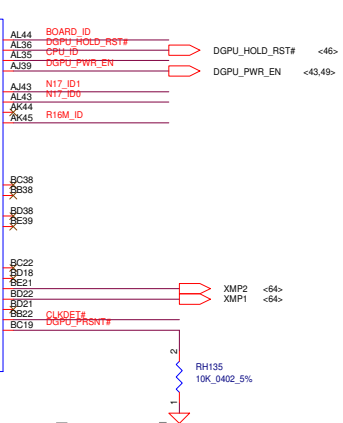



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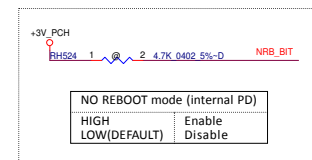
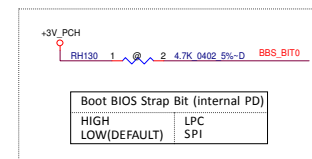




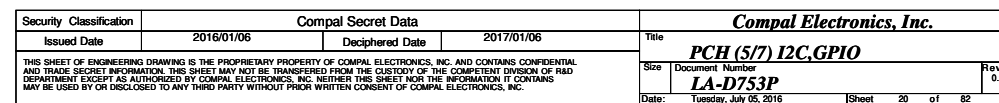




<p>RH25 N17EG3@</p>  <p>S RES 1/20W 10K +5% 0201 SD043100280</p>	<p>RH27 N17EG3@</p>  <p>S RES 1/20W 10K +5% 0201 SD043100280</p>
<p>RH25 N17EG2@</p>  <p>S RES 1/20W 10K +5% 0201 SD043100280</p>	<p>RH28 N17EG2@</p>  <p>S RES 1/20W 10K +5% 0201 SD043100280</p>
<p>RH26 N17EG1@</p>  <p>S RES 1/20W 10K +5% 0201 SD043100280</p>	<p>RH28 N17PG1@</p>  <p>S RES 1/20W 10K +5% 0201 SD043100280</p>



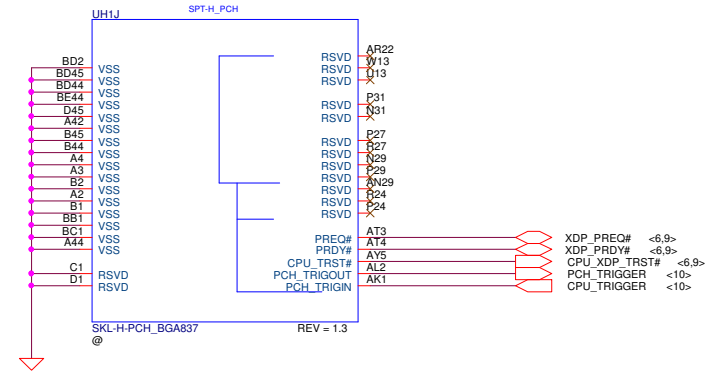
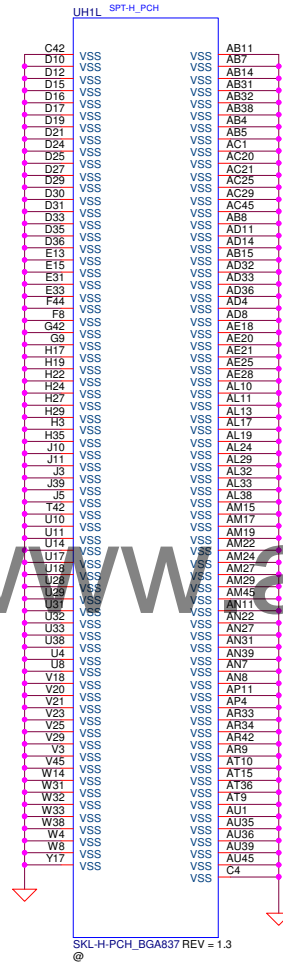
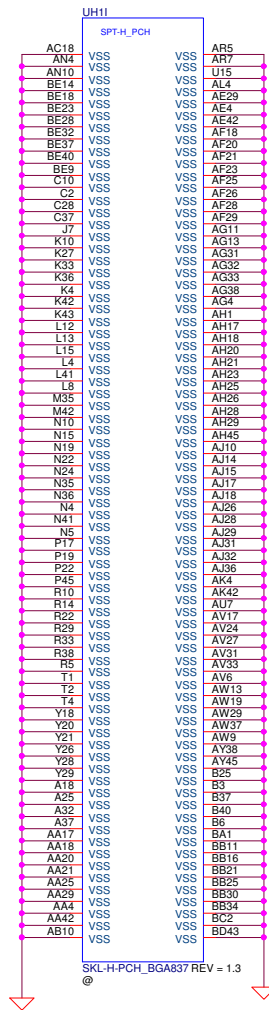
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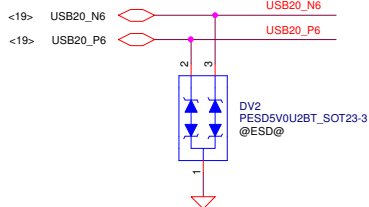
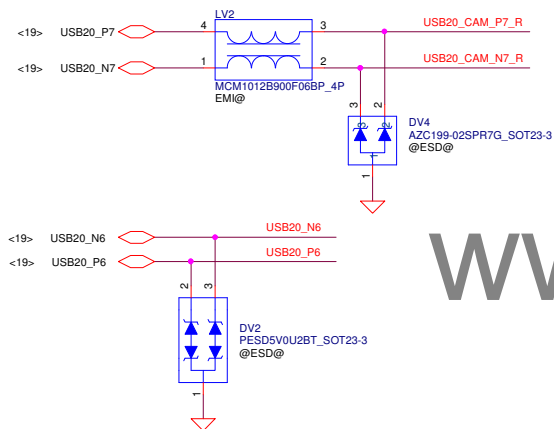
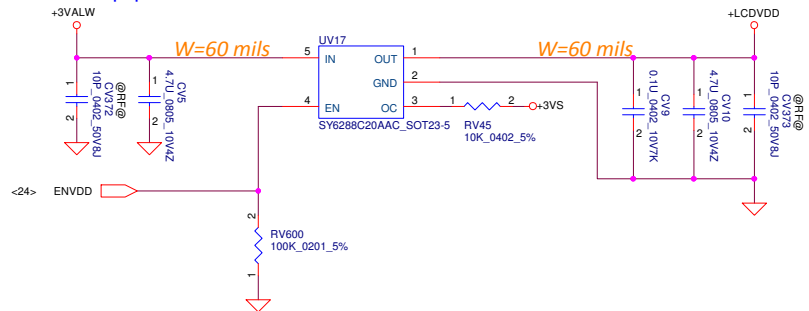
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				Size	Document Number	Rev
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				Date: Tuesday, July 05, 2016		
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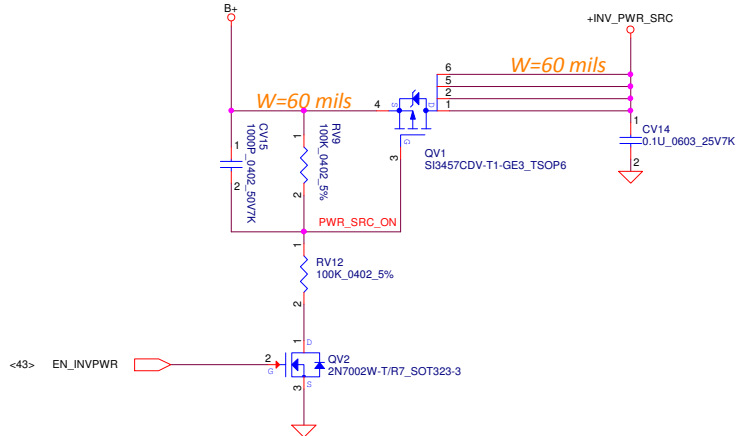
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Issued Date		2016/01/06	Deciphered Date	2017/01/06	
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				Sheet 23 of 82	



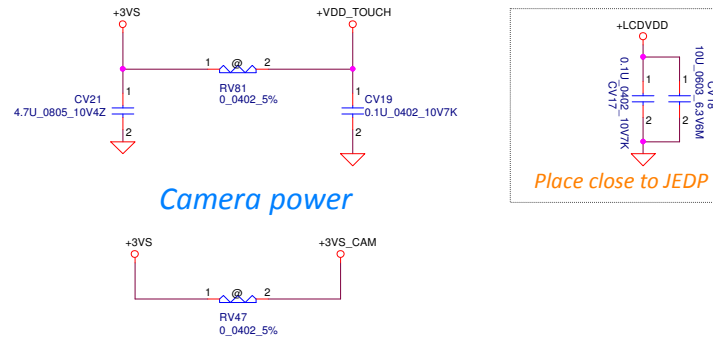
## PCB layout LCD power control



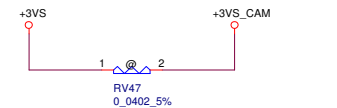
## LCD backlight power control



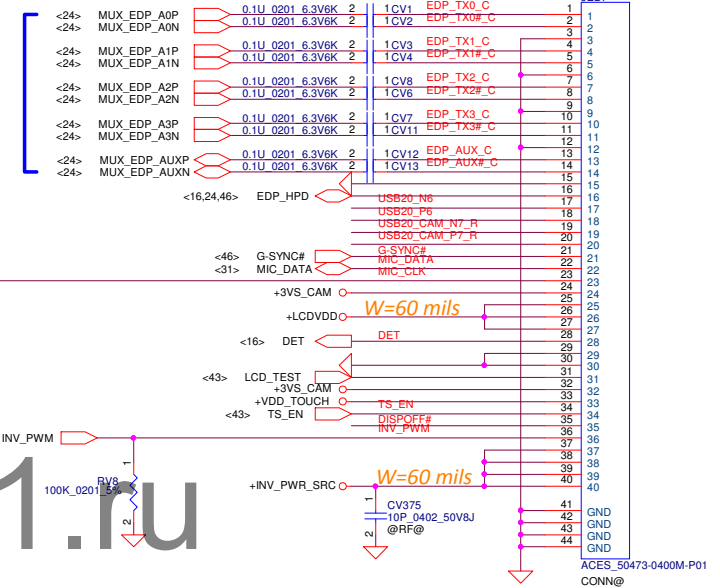
## Touch screen panel power



## Camera power



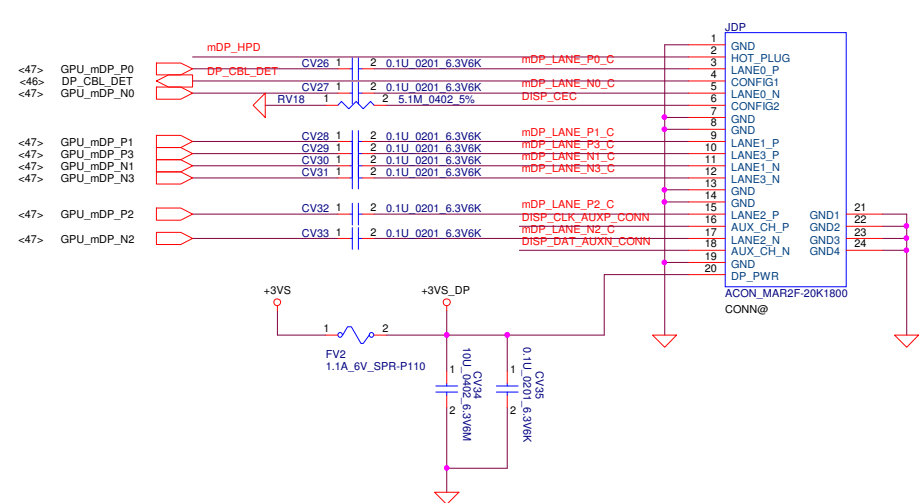
## eDP connector



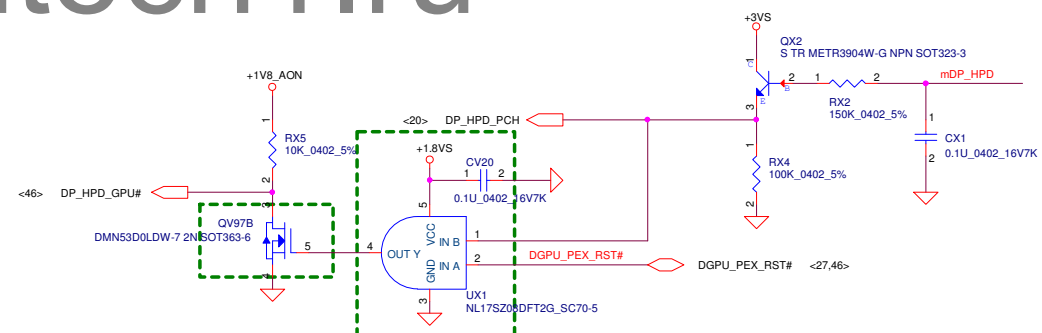
IR camera pindef i ne:  
 IR\_LED+  
 IR\_LED+  
 IR\_LED+/NC  
 IR\_LED-/DET, connect to PCH GPIO  
 IR\_LED-  
 Diglog\_loop, connect to PCH GPIO  
 DGND  
 D+  
 D-  
 USB3V3  
 MIC\_SIG  
 MIC\_CLK  
 DGND

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				Rev	0.2
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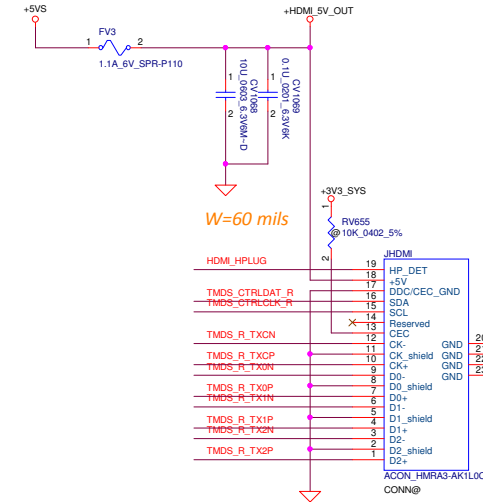
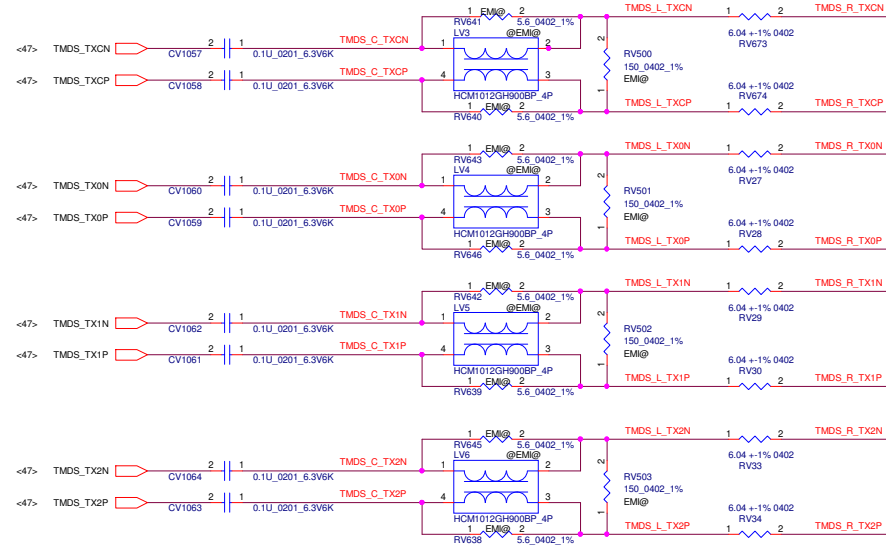


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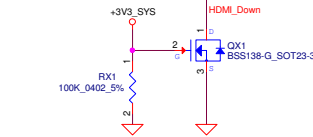
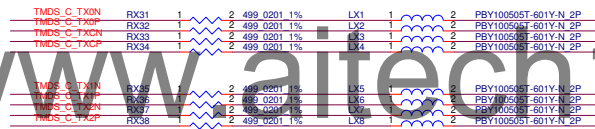


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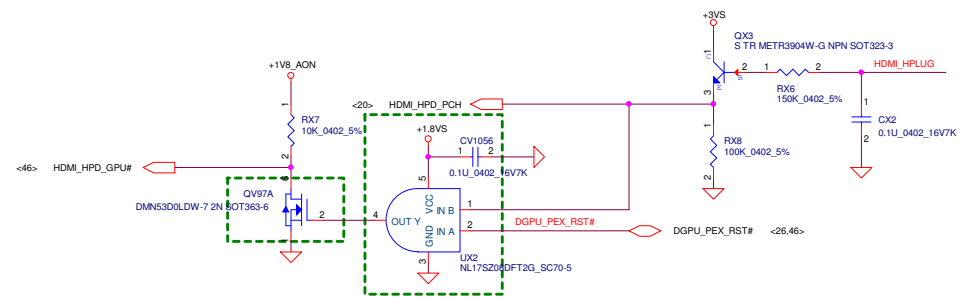
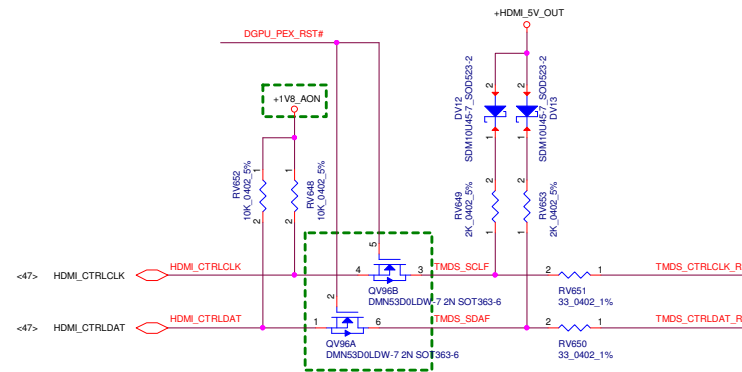
Reserve LV3, LV4, LV5, LV6 co-lay with EMI solution @01/12



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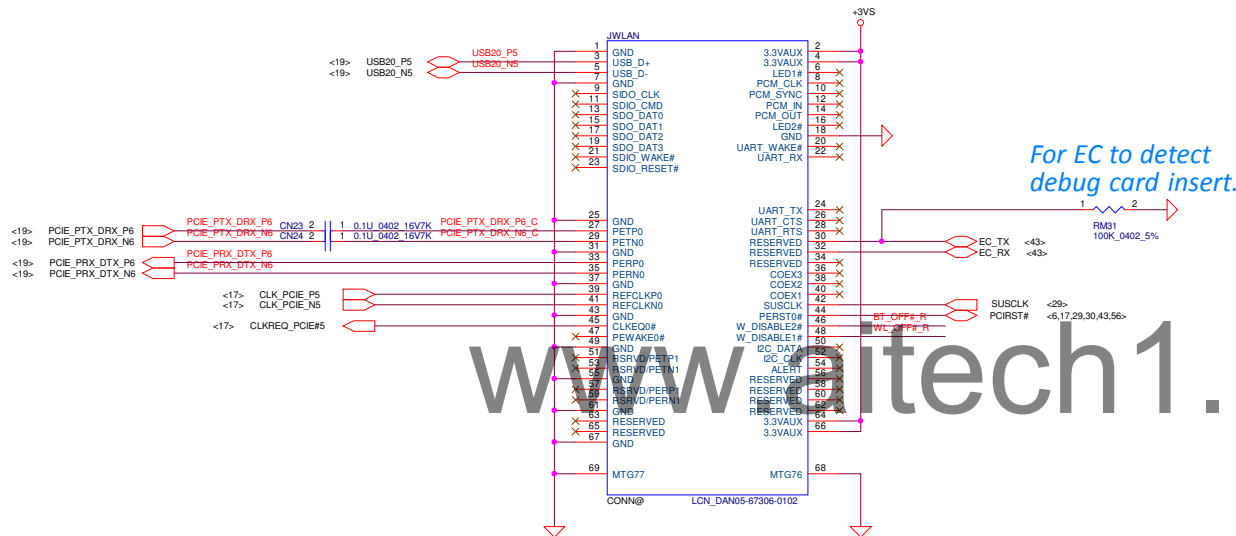


To GPU

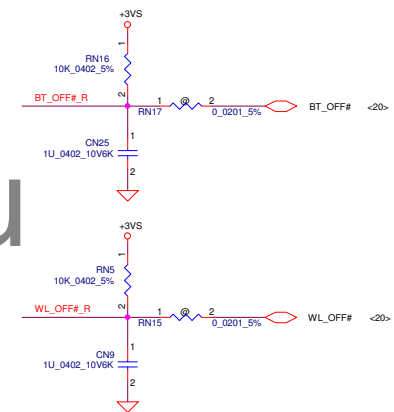


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# M.2 2230 slot(type E)

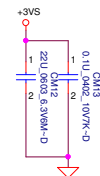


For EC to detect debug card insert.

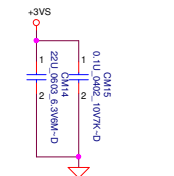


Prevent backdriver from +3VS\_WLAN\_NGFF to +3VS

closed to pin 2, 4



closed to pin 64, 66



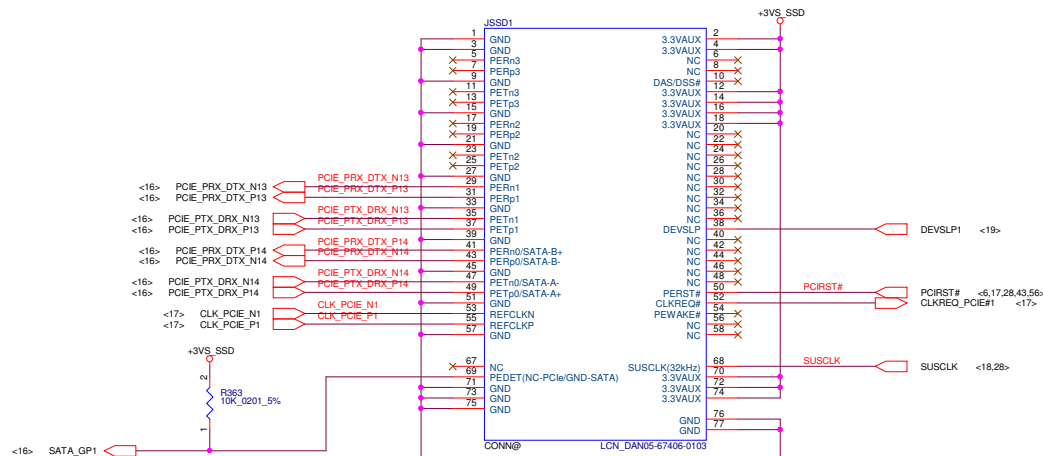
WLAN power control



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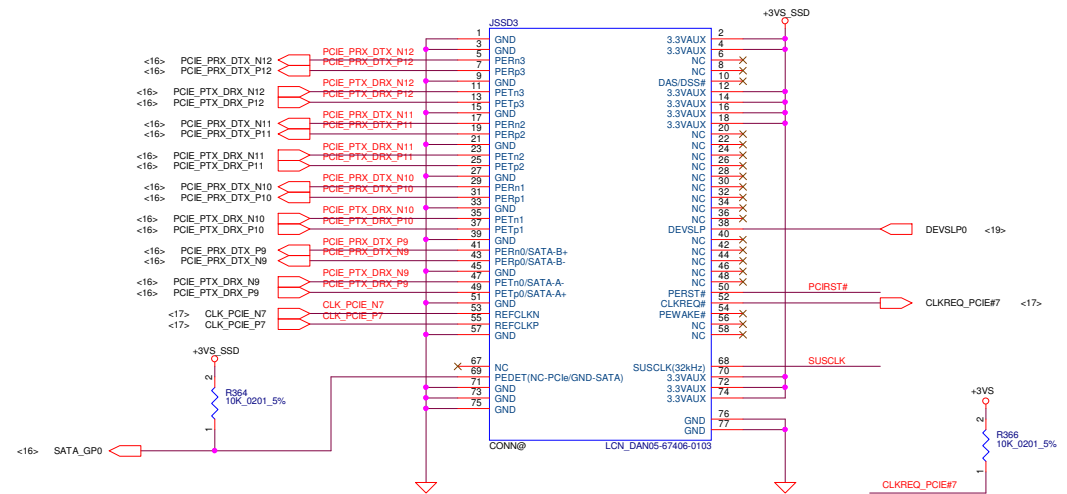


# PCIe/SATA SSD NGFF Slot\_1 Key M

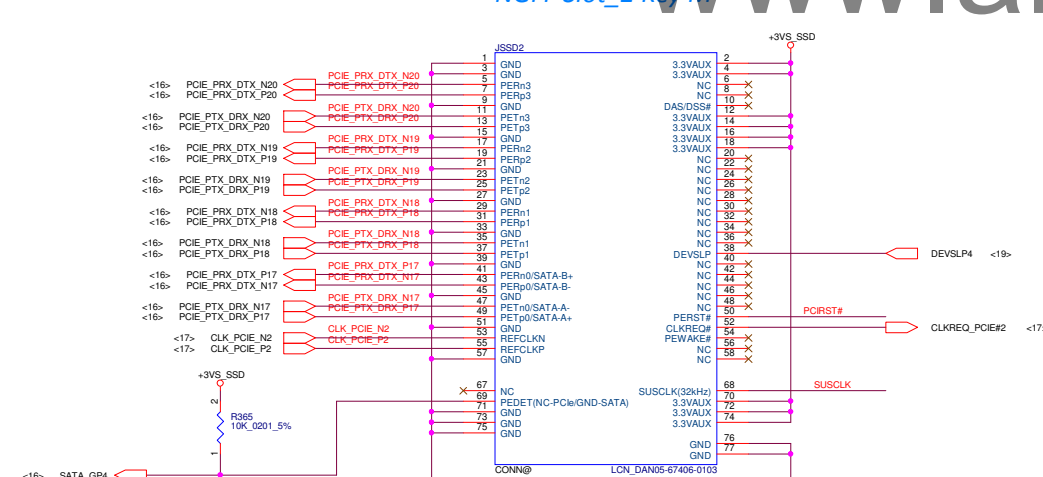


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1	PCIe

# PCIe/SATA SSD NGFF Slot\_3 Key M

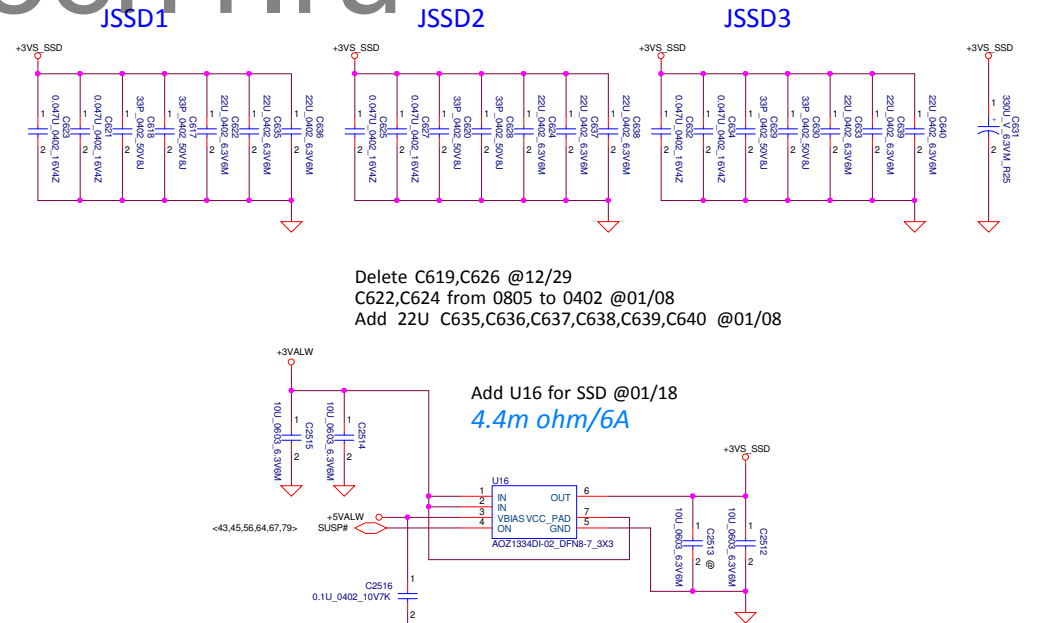


# PCIe/SATA SSD NGFF Slot\_2 Key M

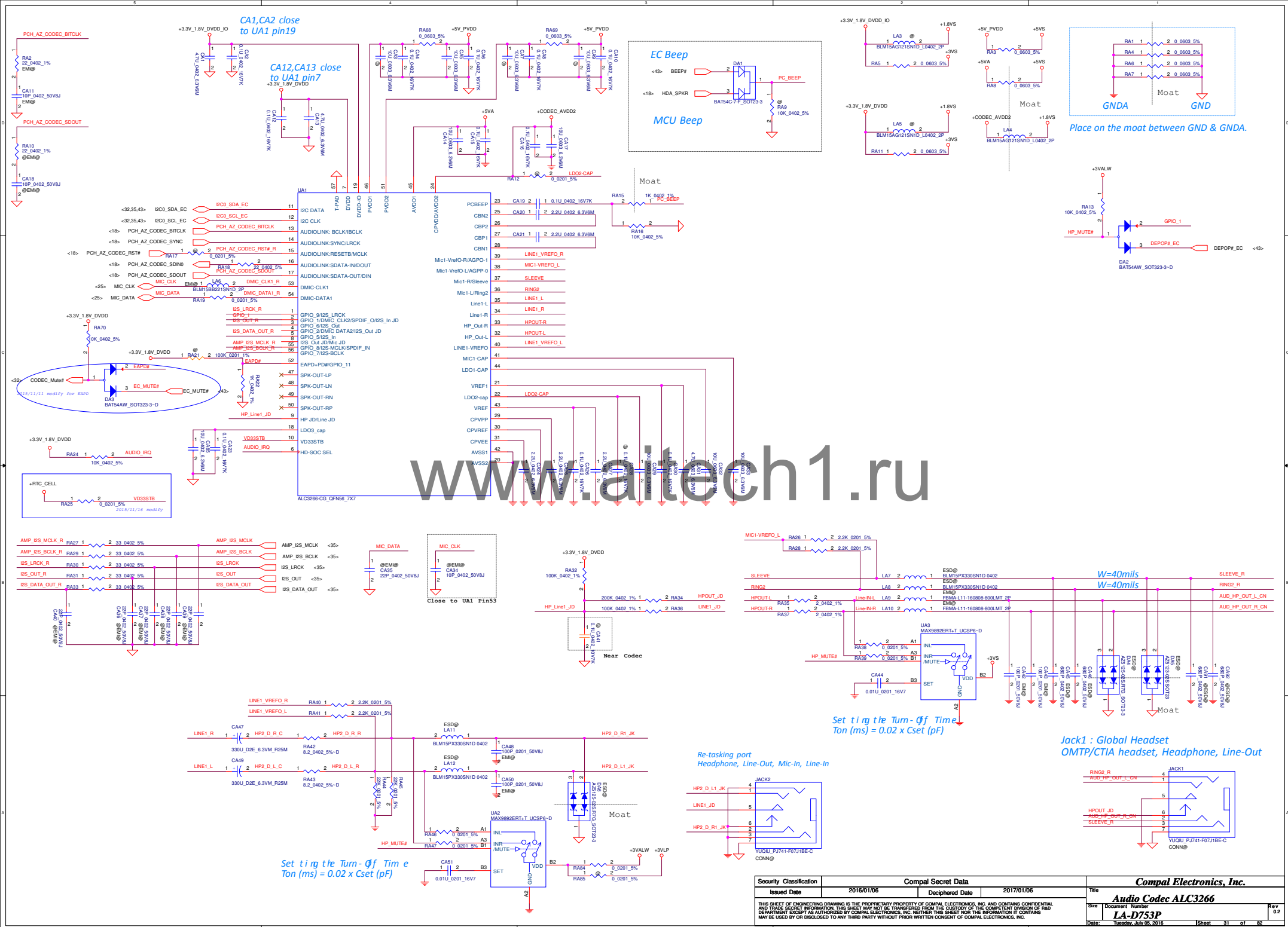


PEDET	Module Type
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1	PCIe

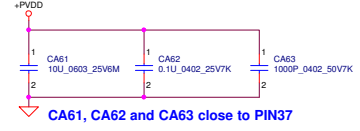
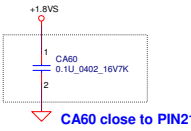
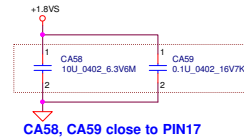
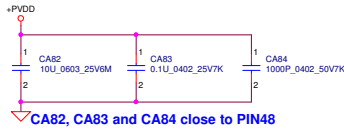
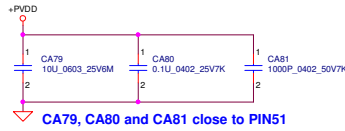
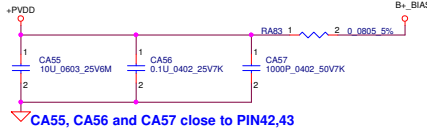
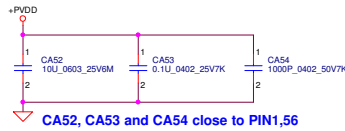
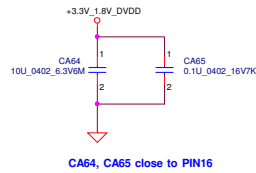
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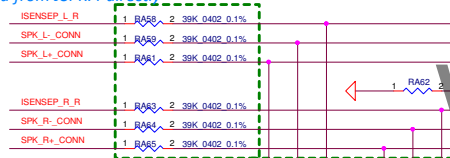




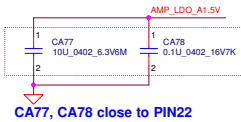
SMART AMP



RA58.1 should from RA57.1 directly  
RA59.1 should from RA57.2 directly  
RA61.1 should from JSPK.4 directly



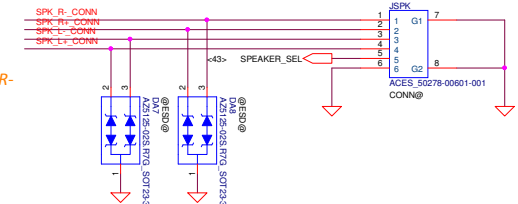
RA63.1 should from RA60.1 directly  
RA64.1 should from RA60.2 directly  
RA65.1 should from JSPK.2 directly



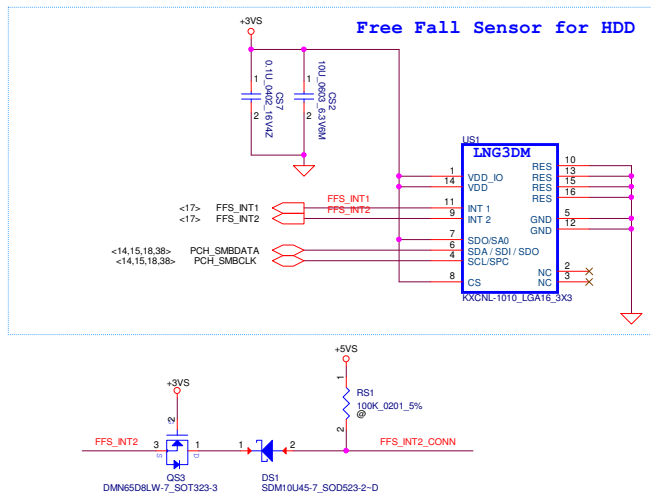
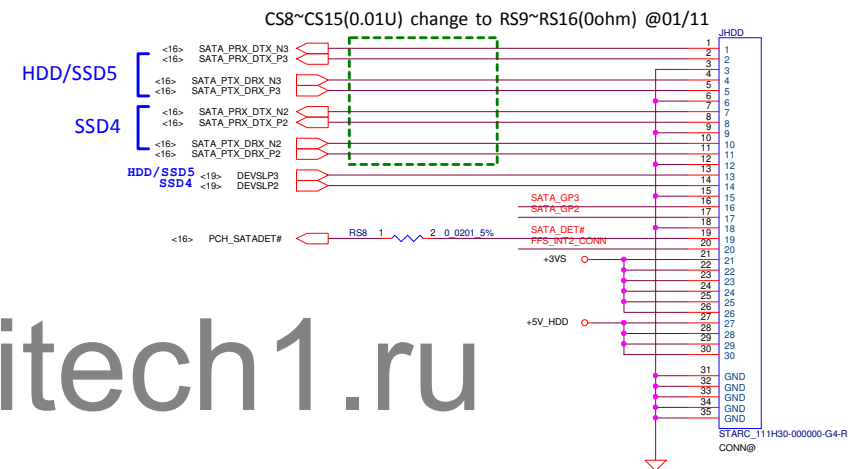
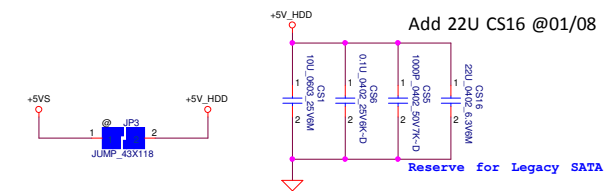
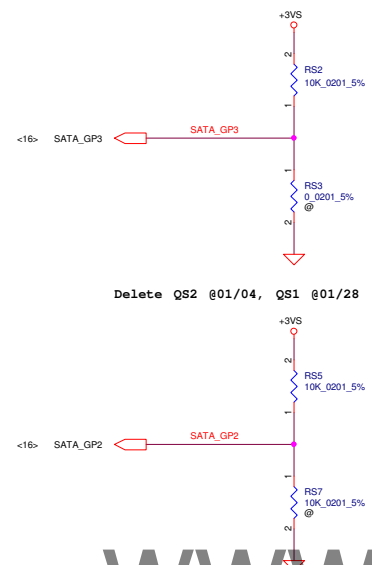
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Int. Speaker Conn.

40 mils = For 4 ohm 3W Speaker  
Close to UA1 Pin42,43,44,45

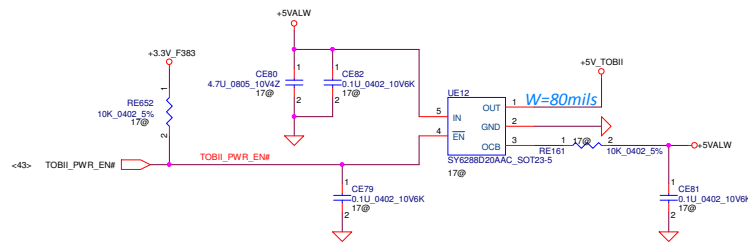


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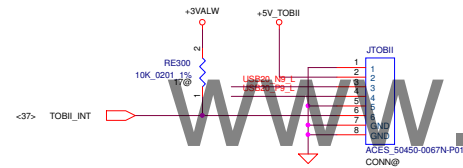
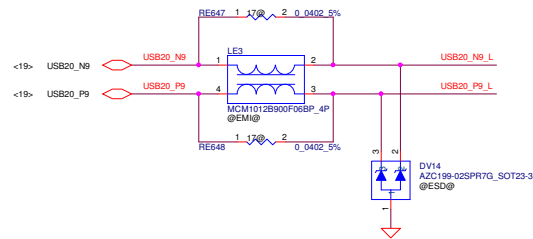


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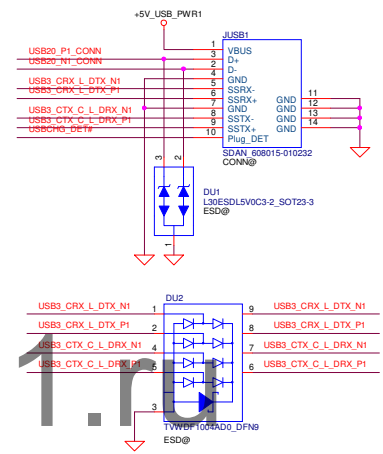
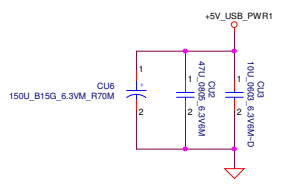
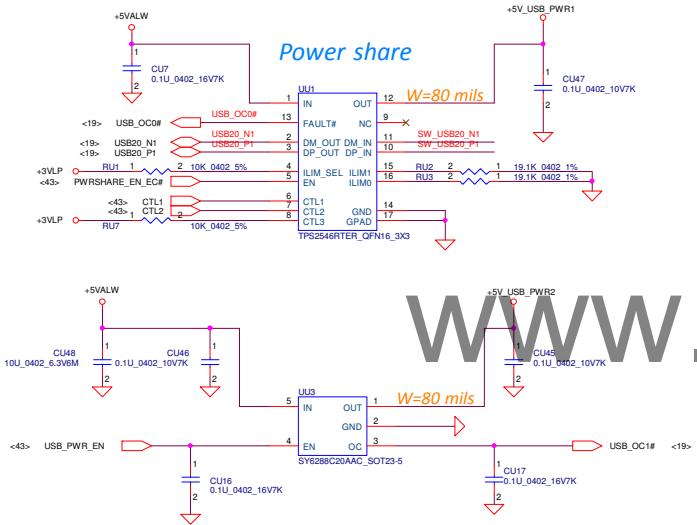
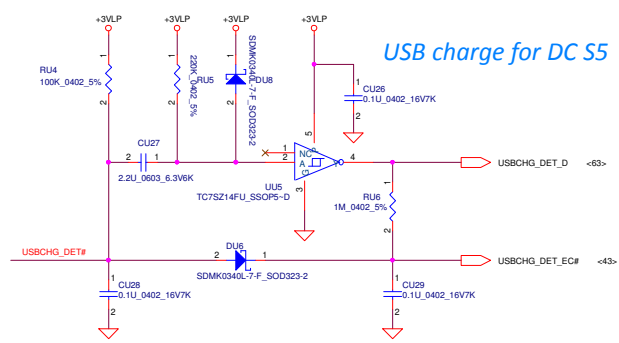
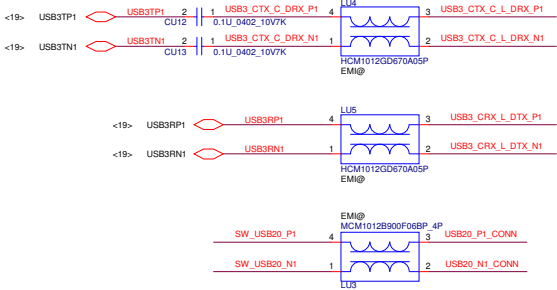
**Tobii Conn.**



*Near JTOBII*

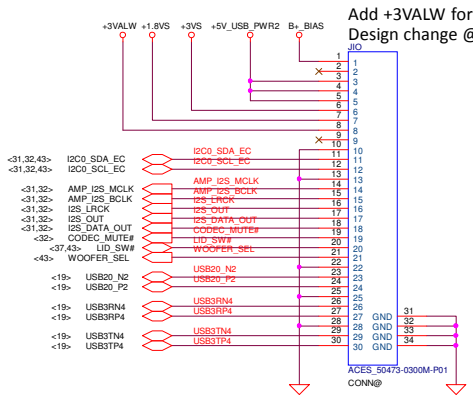
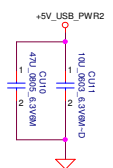


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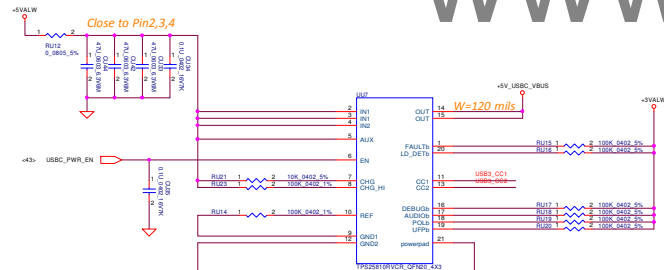
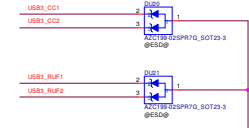
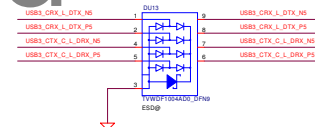
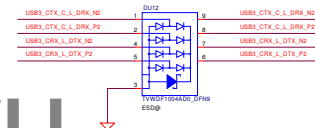
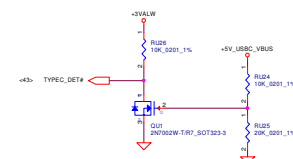
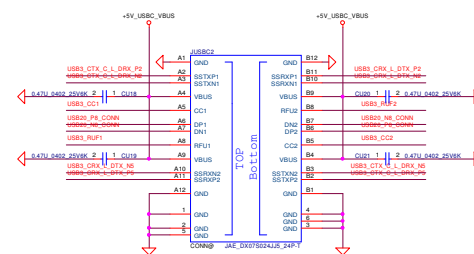
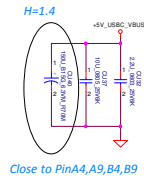
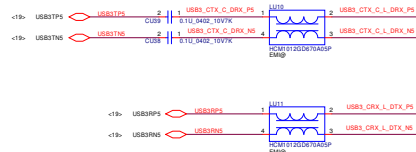
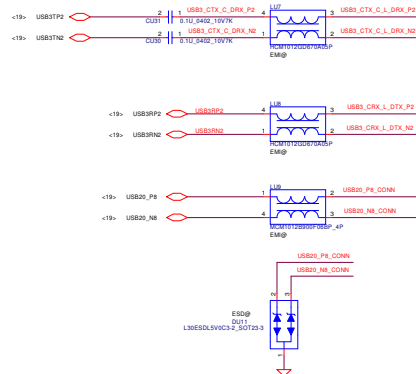


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		Date:		Tuesday, July 05, 2016	
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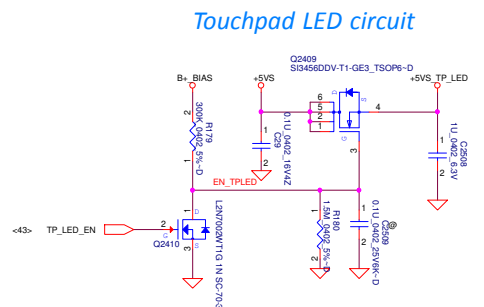
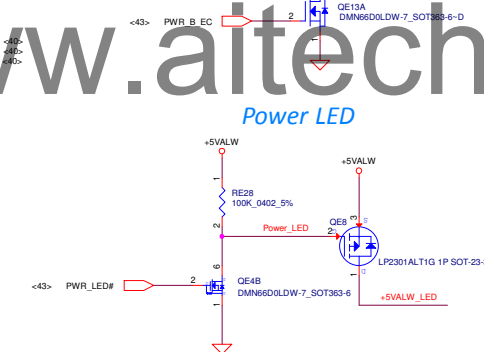
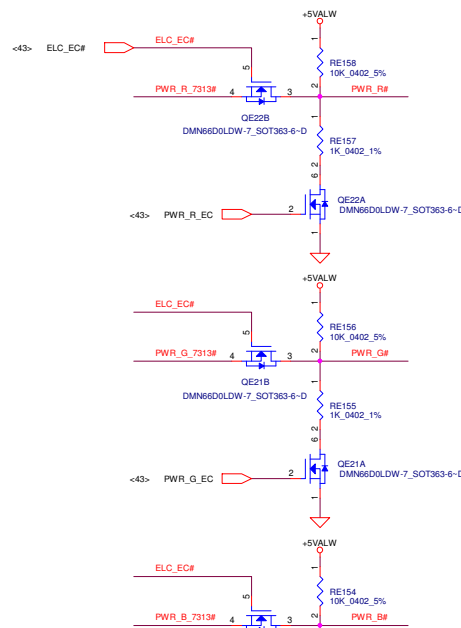
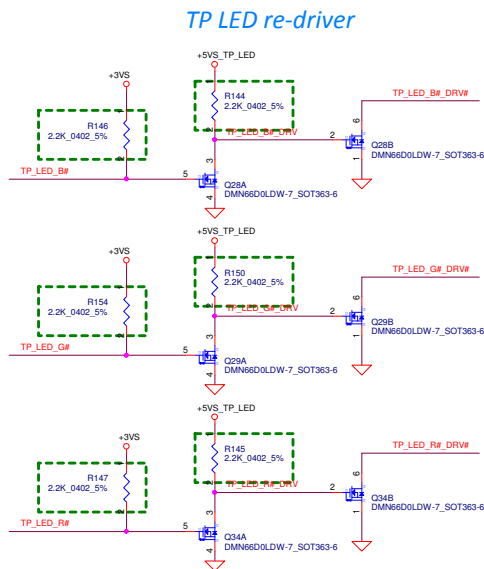
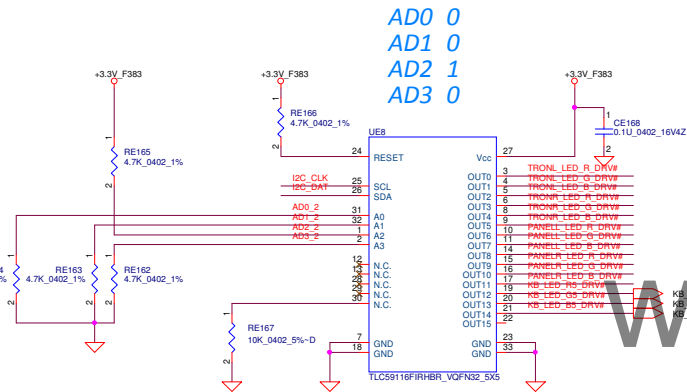
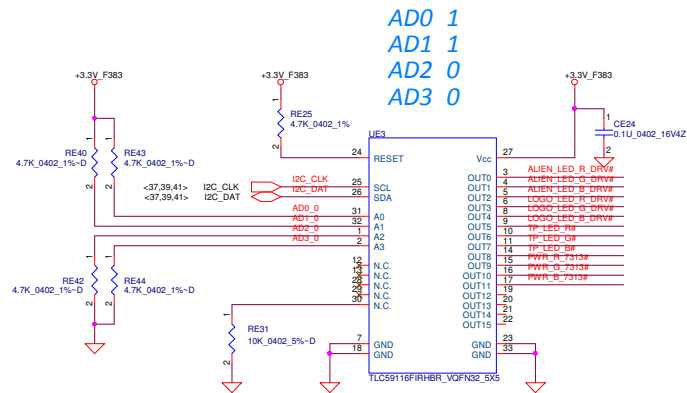


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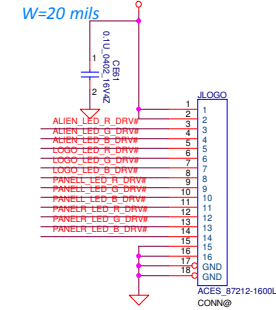
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				Page	1 of 1



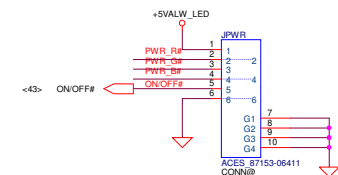




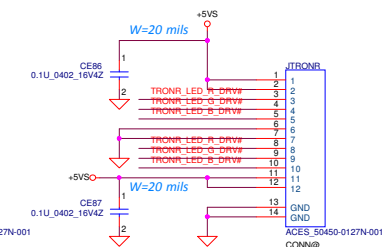
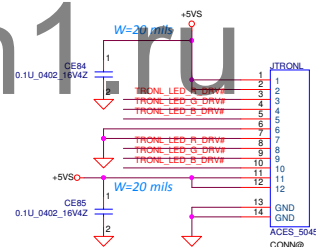
**To logo board**  
Change connector from 14pin to 16pin @12/16



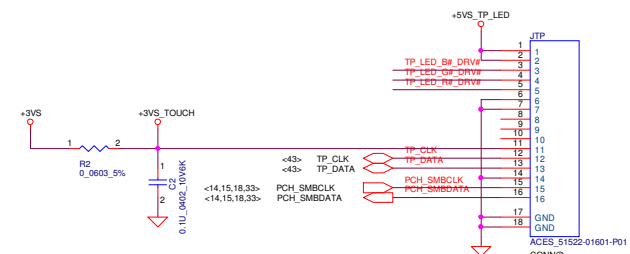
**To power board**



**To Tron Light board X2**  
Change connector from 6pin\*4 to 12pin\*2 @12/16



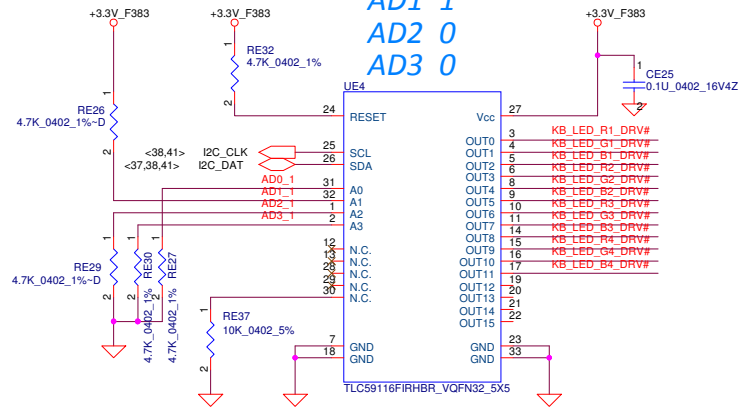
**To touchpad module**



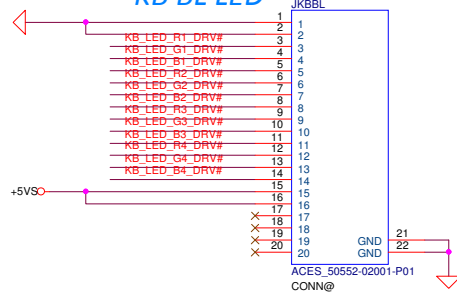
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2016/01/06		2017/01/06		ELC (2) TP/PW/LOGO/TRON	
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2016/01/06		2017/01/06		Rev 0.2	
2016/01/06		2017/01/06		LA-D753P	

## KB Backlight

AD0 0  
AD1 1  
AD2 0  
AD3 0



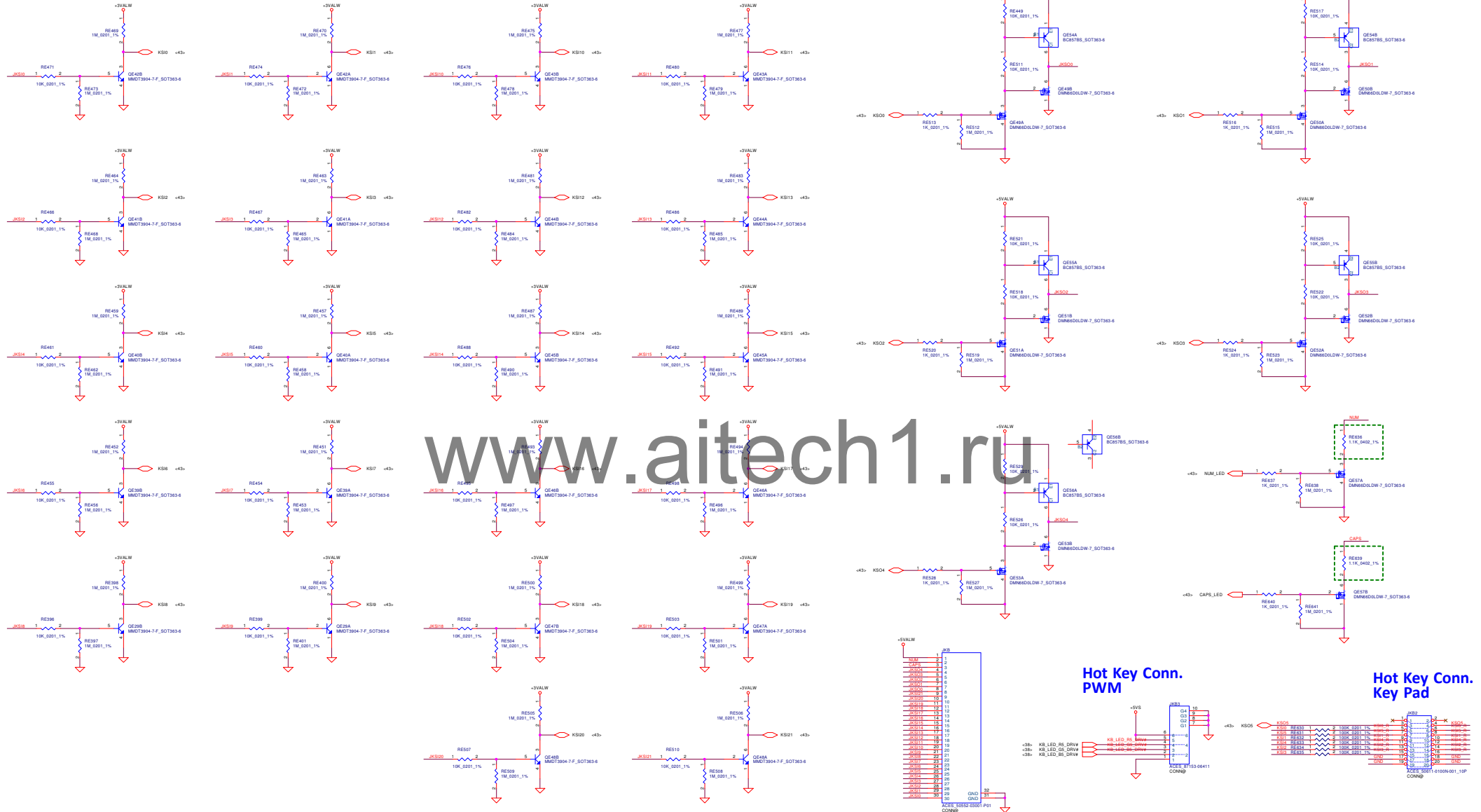
## KB BL LED



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	ELC (3) KBBL
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				Date	Rev
				Tuesday, July 05, 2016	0.2
				Sheet	39 of 82

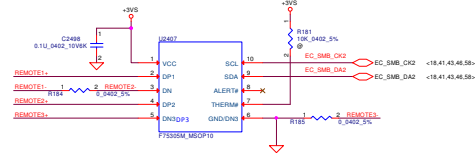
QE54, QE55, QE56 change to SB000018700



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Issued Date	2016/01/06	Designed Date	2017/01/06	Ver	ELC(4) NKRO KB
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Doc No	LA-D753P	Rev	0.1	Part No	LA-D753P
Issue	1	Date	2017.01.06	Drawn	01

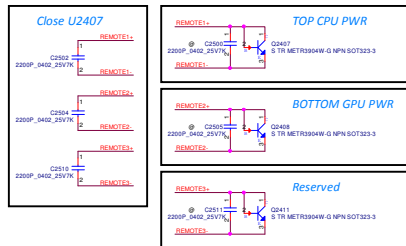


Fintek thermal sensor----> CPU core, DIMM



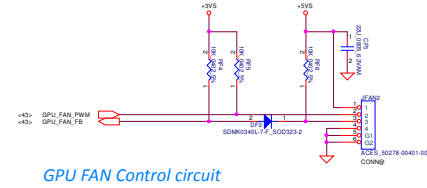
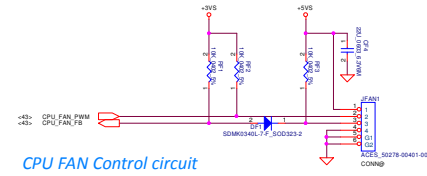
Address 1001\_101xb

2nd source  
SA000029210-->EMC1403-2-AIZL-TR



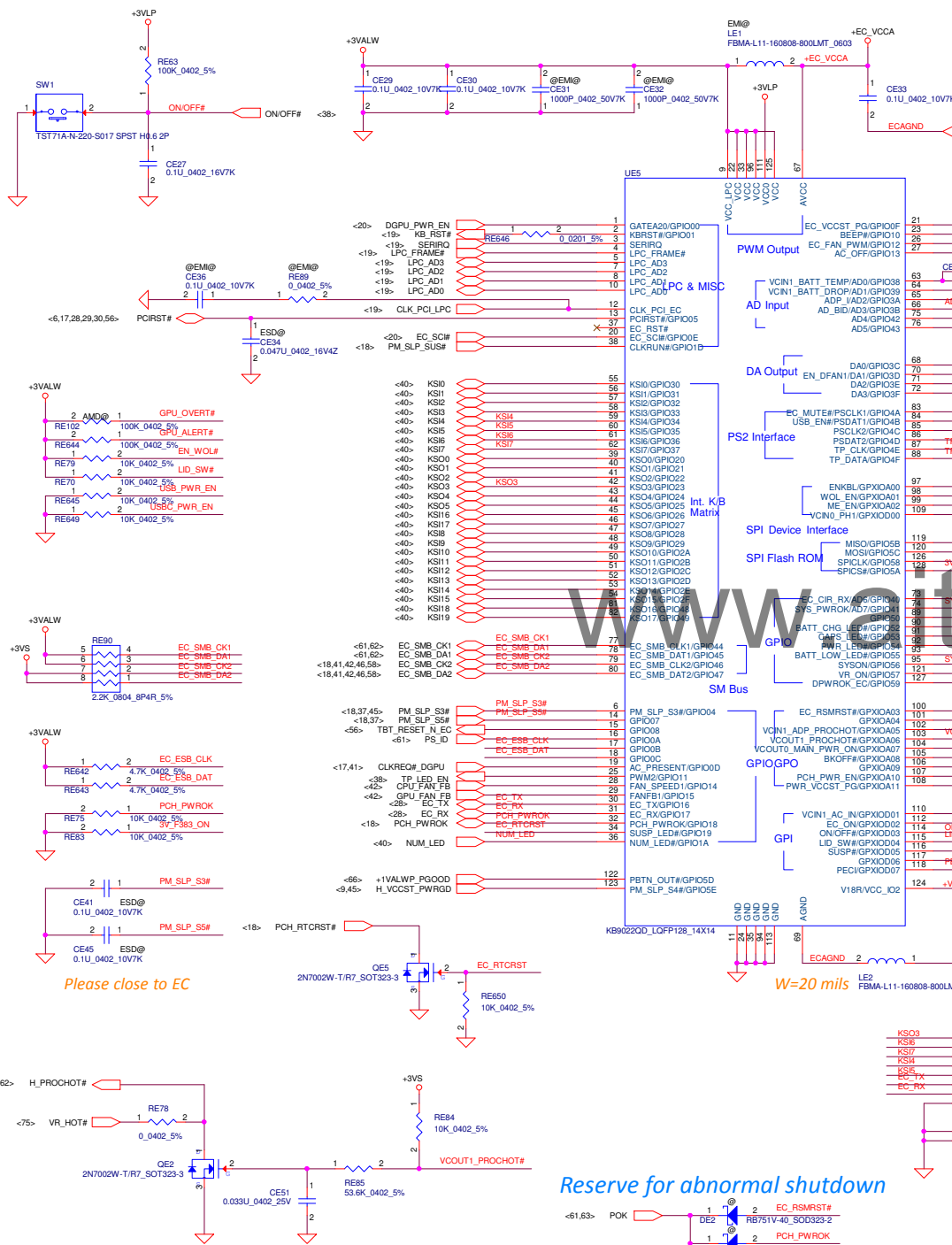
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REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8



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Issued Date	2016/01/06	Designated Date	2017/01/06	Title	FAN/Thermal
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				Checked	2016/01/06
				Approved	2016/01/06

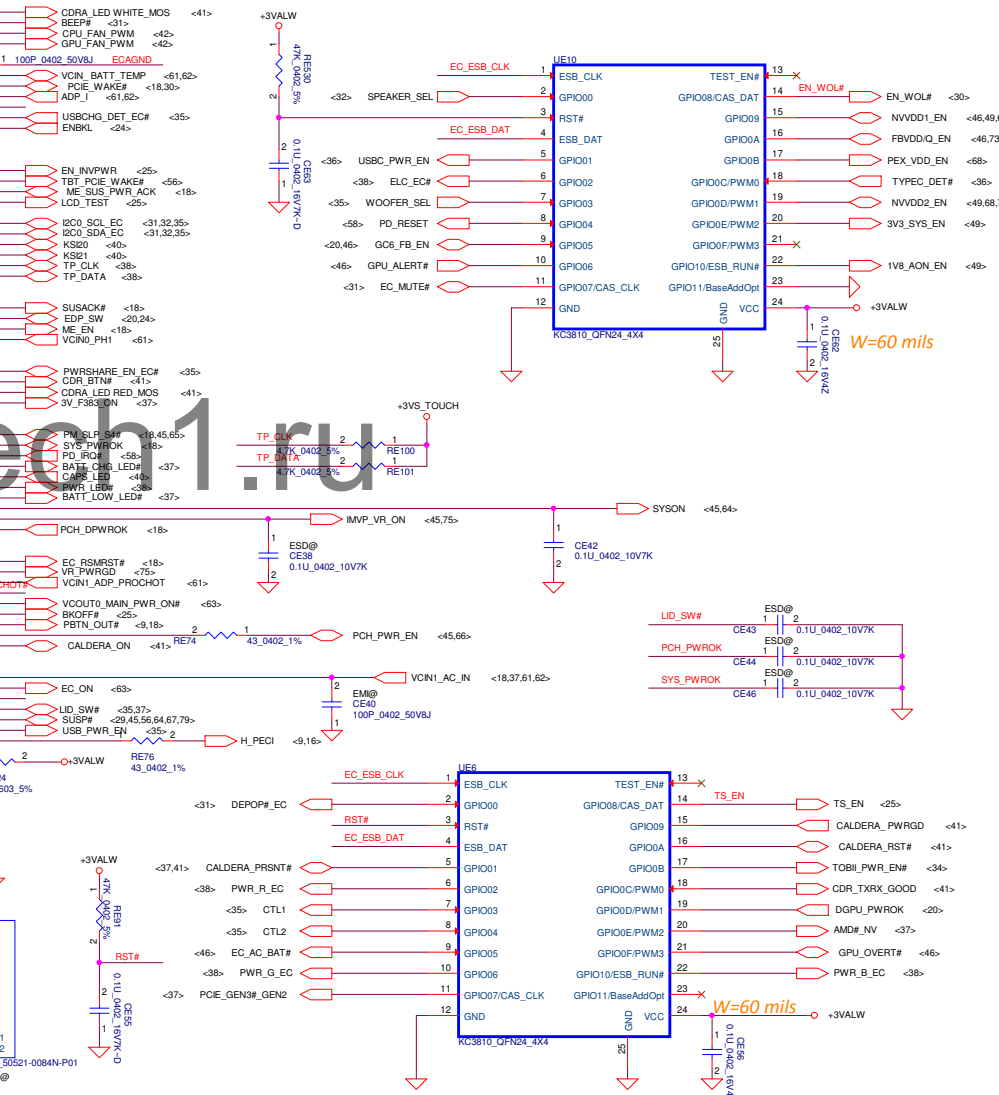
## Power ON circuit



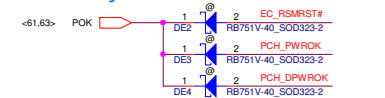
01.SD034120280	12K	0.402	1%
02.SD034150280	15K	0.402	1%
03.SD028200280	20K	0.402	1%
04.SD034270280	27K	0.402	1%
05.SD034330280	33K	0.402	1%
06.SD034430280	43K	0.402	1%
07.SD034560280	56K	0.402	1%
08.SD034750280	75K	0.402	1%
09.SD034100380	100K	0.402	1%
10.SD034130380	130K	0.402	1%
11.SD034160380	160K	0.402	1%
12.SD034200380	200K	0.402	1%
13.SD000001880	240K	0.402	1%
14.SD000006280	270K	0.402	1%
15.SD034330380	330K	0.402	1%
16.SD028430380	430K	0.402	1%
17.SD034560300	560K	0.402	1%
18.SD00000AL80	750K	0.402	1%

## DVT1-build

## Board ID

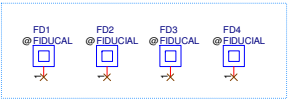


## Reserve for abnormal shutdown

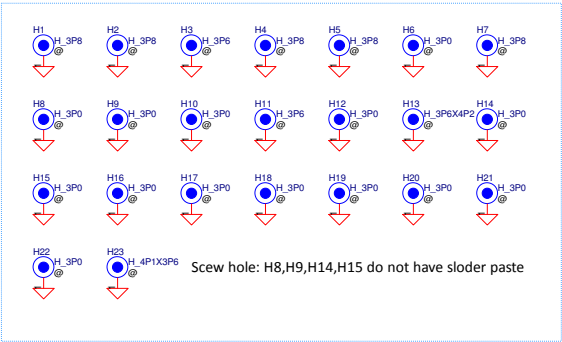


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		LA-D753P	Rev 0.2
		Date	Tuesday, July 05, 2016
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Fiducial Mark



PCB Screw Hole

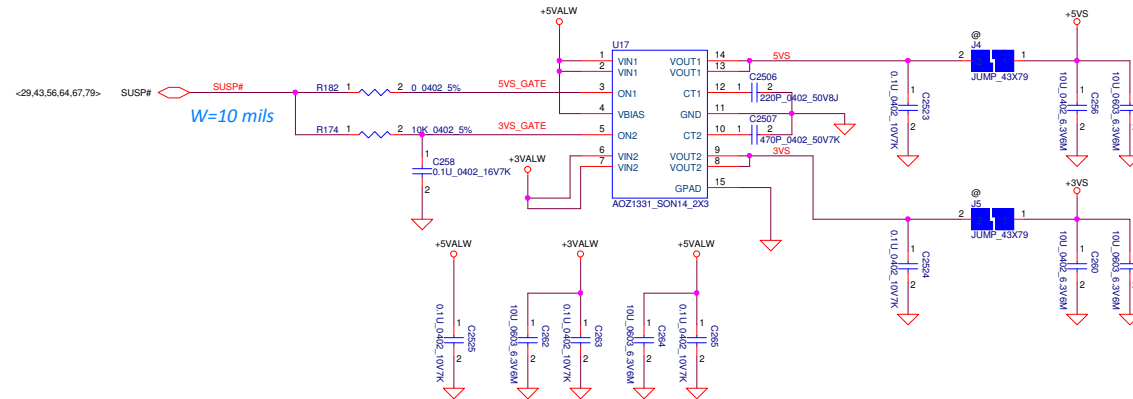


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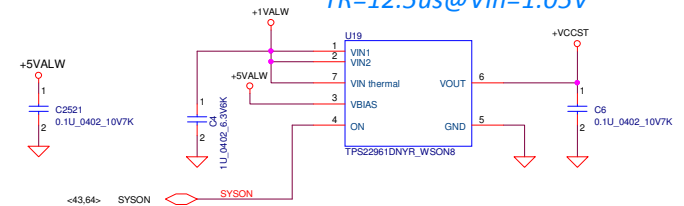
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2016/01/06	Deciphered Date	2017/01/06	Title
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		LA-D753P			0.2
		Date: Tuesday, July 05, 2016			Sheet 44 of 82



+5VS and +3VS switch  
20mohm/6A per channel



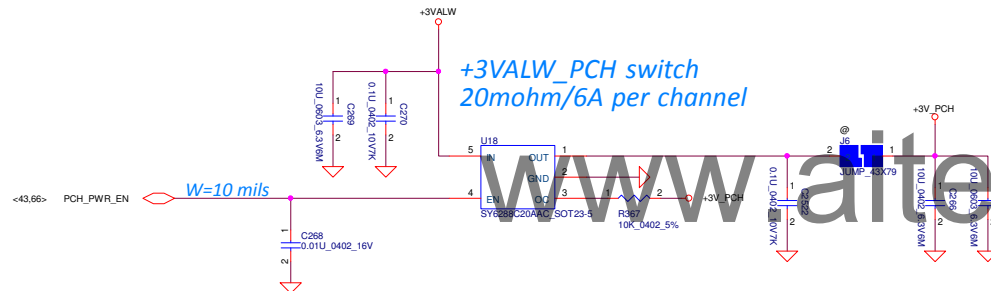
+VCCST switch  
4.4mohm/6A  
TR=12.5us@Vin=1.05V



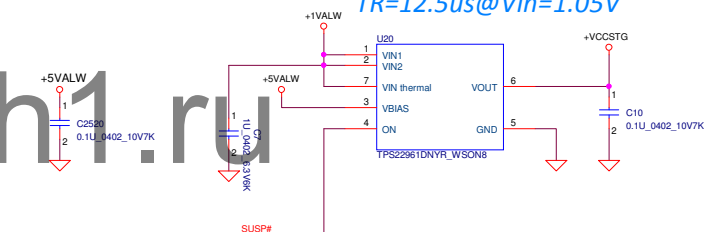
Main source  
2nd source  
3rd source  
4st source

TI SA00007XR00 (SI C TPS22961DNYR V8 ON 8P LOADS WTC)  
ACS SA00008A800 (SI C ACZ1334D-01 DF N 8P 9 NGLE LOADS W  
E MC SA00008R600 (SI C E M201V DF NBX3 8P LOADS WTC)  
APEC SA00006V300 (SI C APE8939GNB DF N 8P LOADS WTC)

+3VALW\_PCH switch  
20mohm/6A per channel



+VCCSTG switch  
4.4mohm/6A  
TR=12.5us@Vin=1.05V



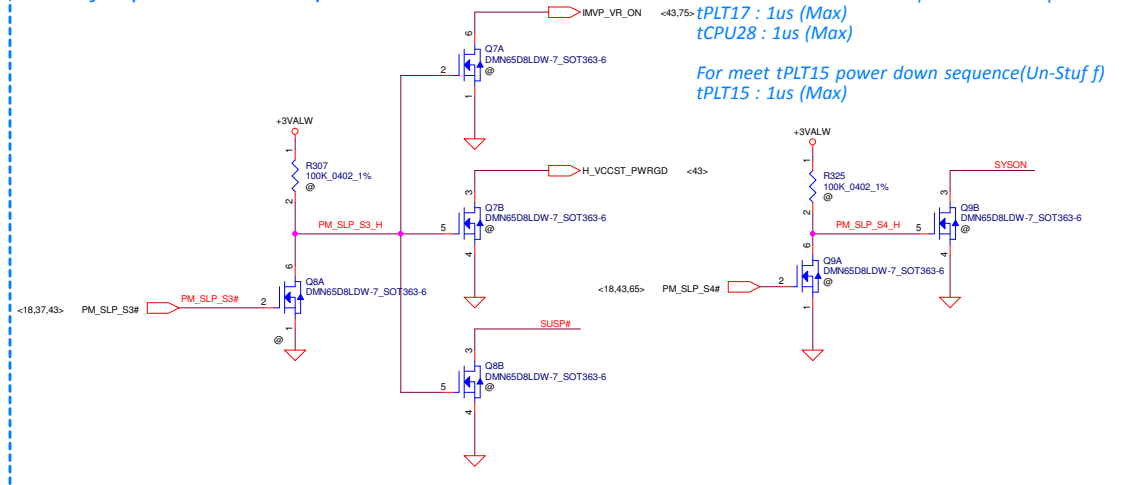
Main source  
2nd source  
3rd source  
4st source

TI SA00007XR00 (SI C TPS22961DNYR V8 ON 8P LOADS WTC)  
ACS SA00008A800 (SI C ACZ1334D-01 DF N 8P 9 NGLE LOADS W  
E MC SA00008R600 (SI C E M201V DF NBX3 8P LOADS WTC)  
APEC SA00006V300 (SI C APE8939GNB DF N 8P LOADS WTC)

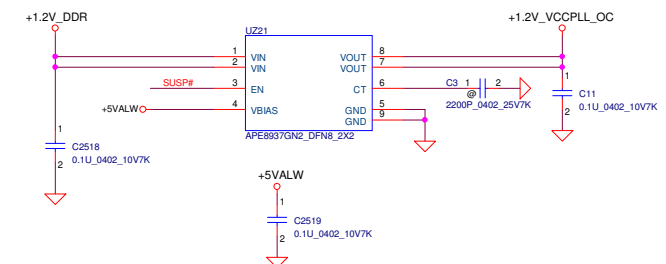
add for power down sequence

For meet tPLT17 & tCPU28 power down sequence.  
tPLT17 : 1us (Max)  
tCPU28 : 1us (Max)

For meet tPLT15 power down sequence(Un-Stuf f)  
tPLT15 : 1us (Max)

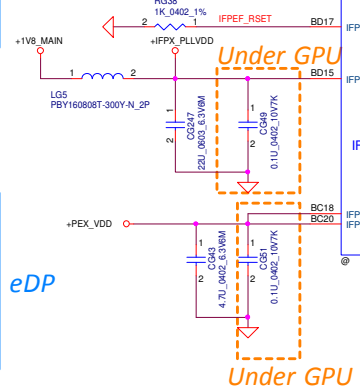
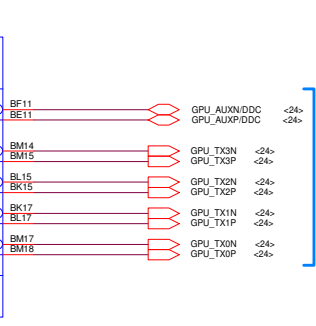
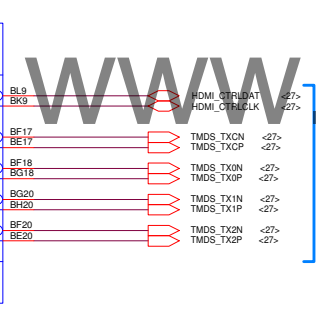
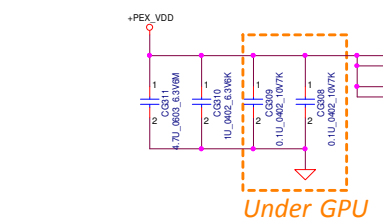
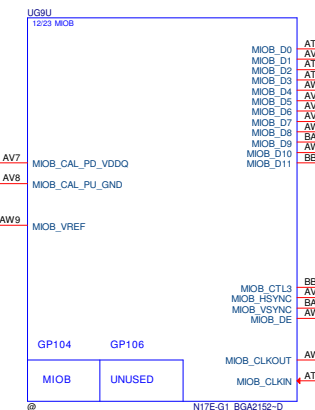


+1.2V\_VCCPLL\_OC switch  
22mohm/4A  
TR=520us@Vin=0.8V

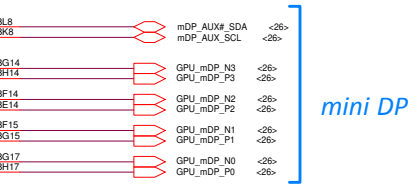
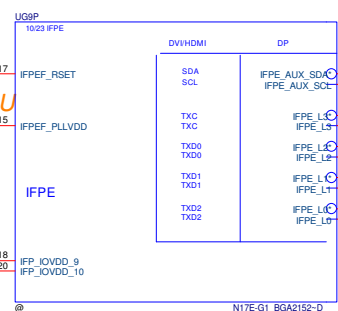


Security Classification		Compal Secret Data		Title	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	DC/DC Interface	
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				LA-D753P	Rev 0.2
				Date	Tuesday, July 05, 2016
				Sheet	45 of 82



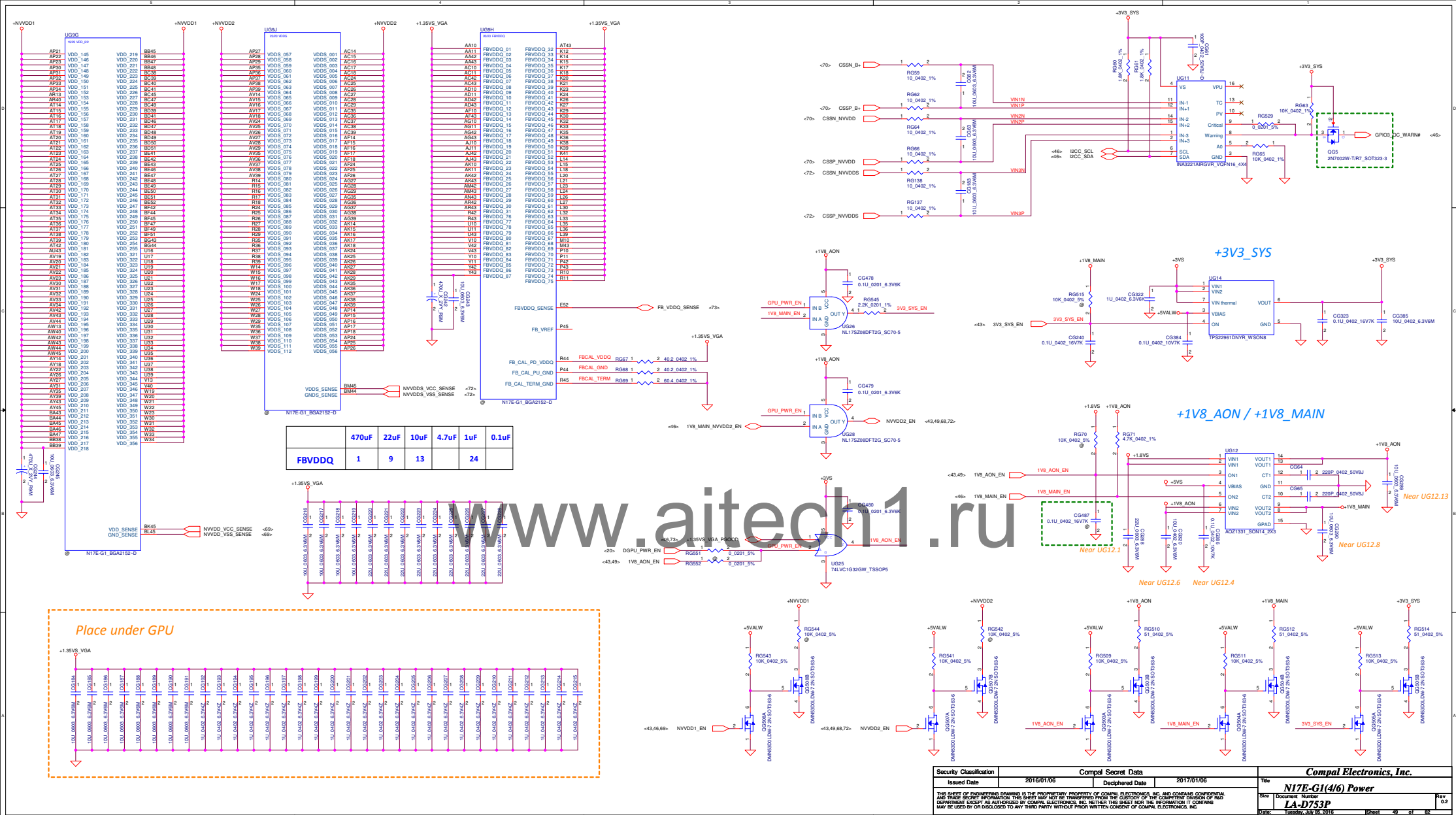


	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			2		4
IFPx_PLLVDD	1				2





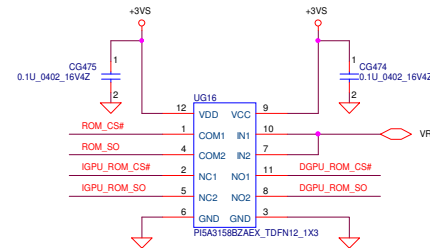
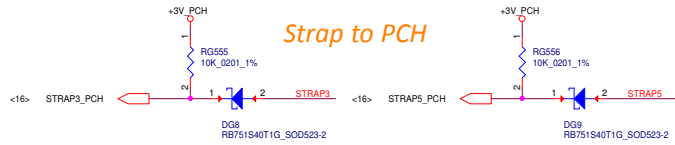
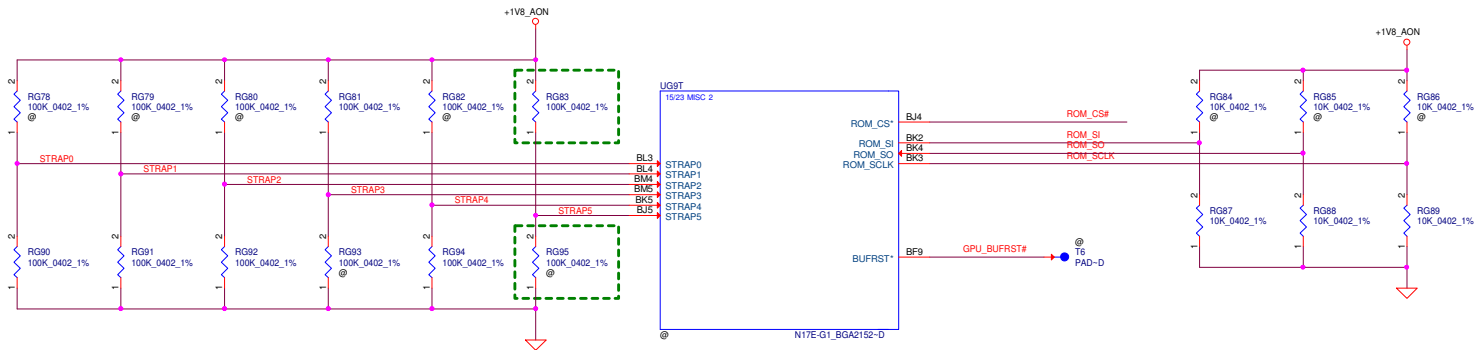
<b>N17E-G1(3/6) MEM Interface</b>	
Size	Document Number
	<b>LA-D753P</b>
Date	Version 1.1/06/2002



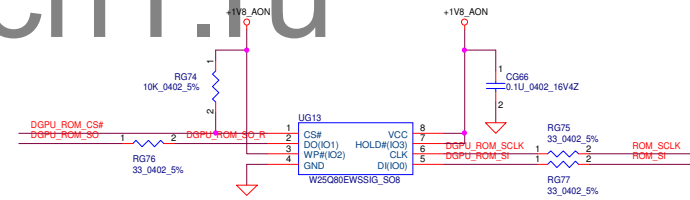
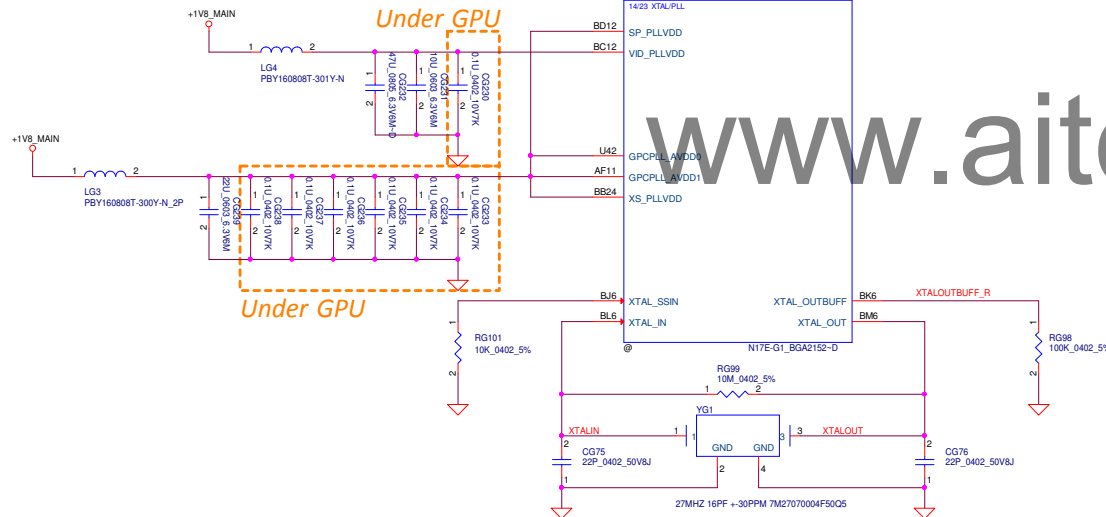




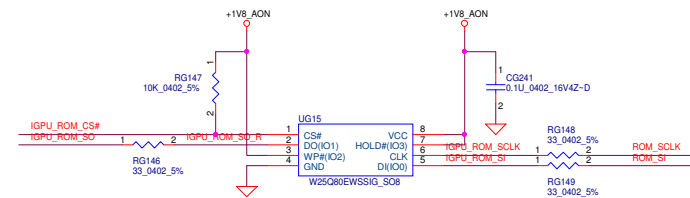
	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD		1				
GPCPLL_AVDD						6



Function	VROM_SEL
COM = NC	L
COM = NO	H

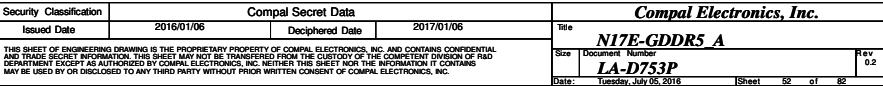


DGPU VBIOS ROM

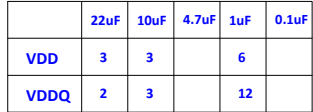


Opt i ms VB OS ROM

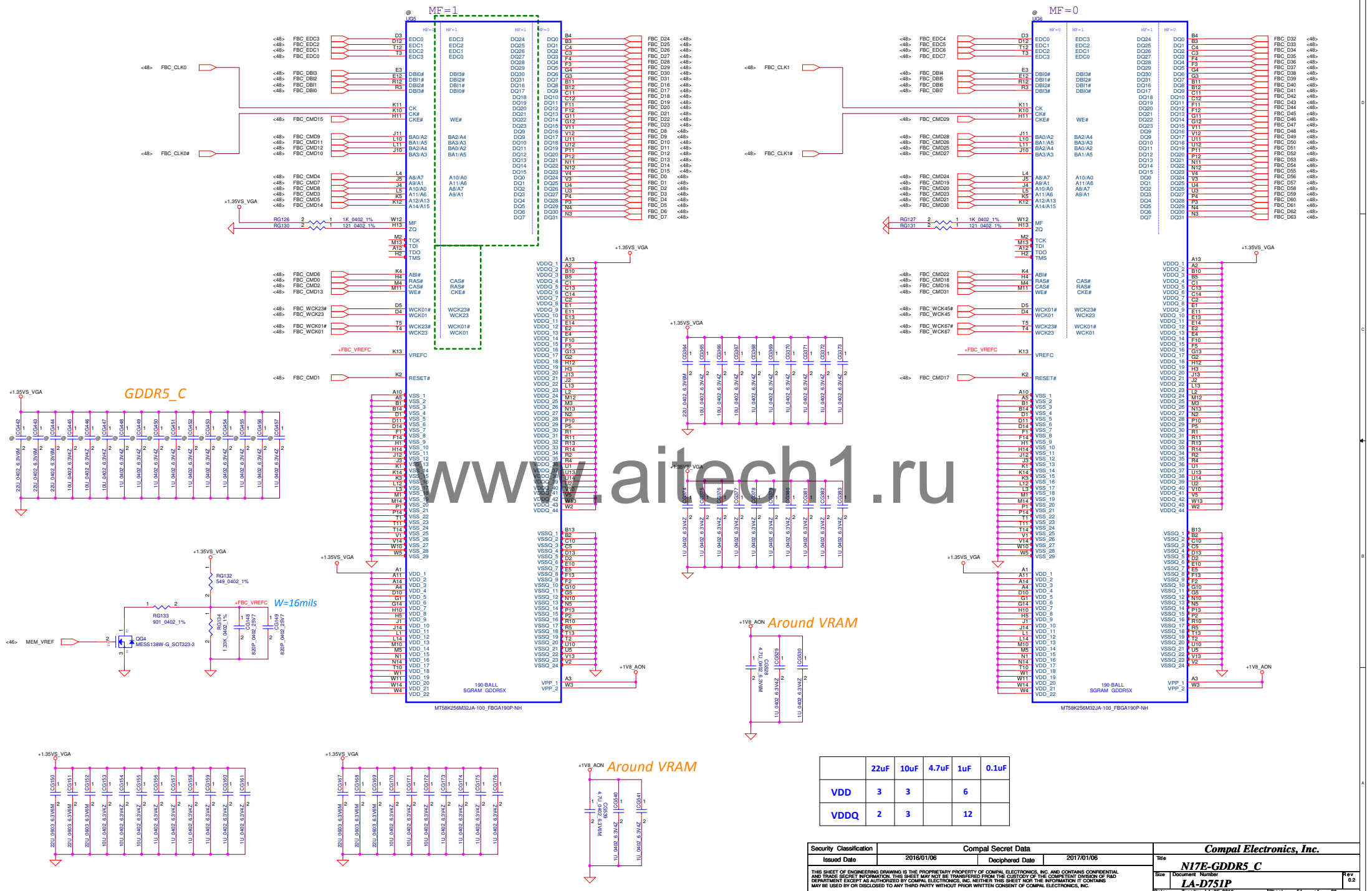
GDDR5x VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
Micron , MT58K256M32	L	L	L	H	L	L	0
	H	L	L	H	L	L	1
	L	H	L	H	L	L	2



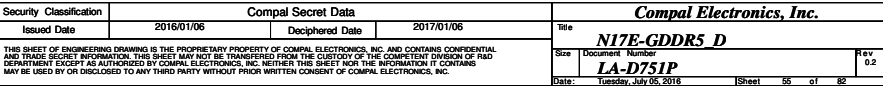


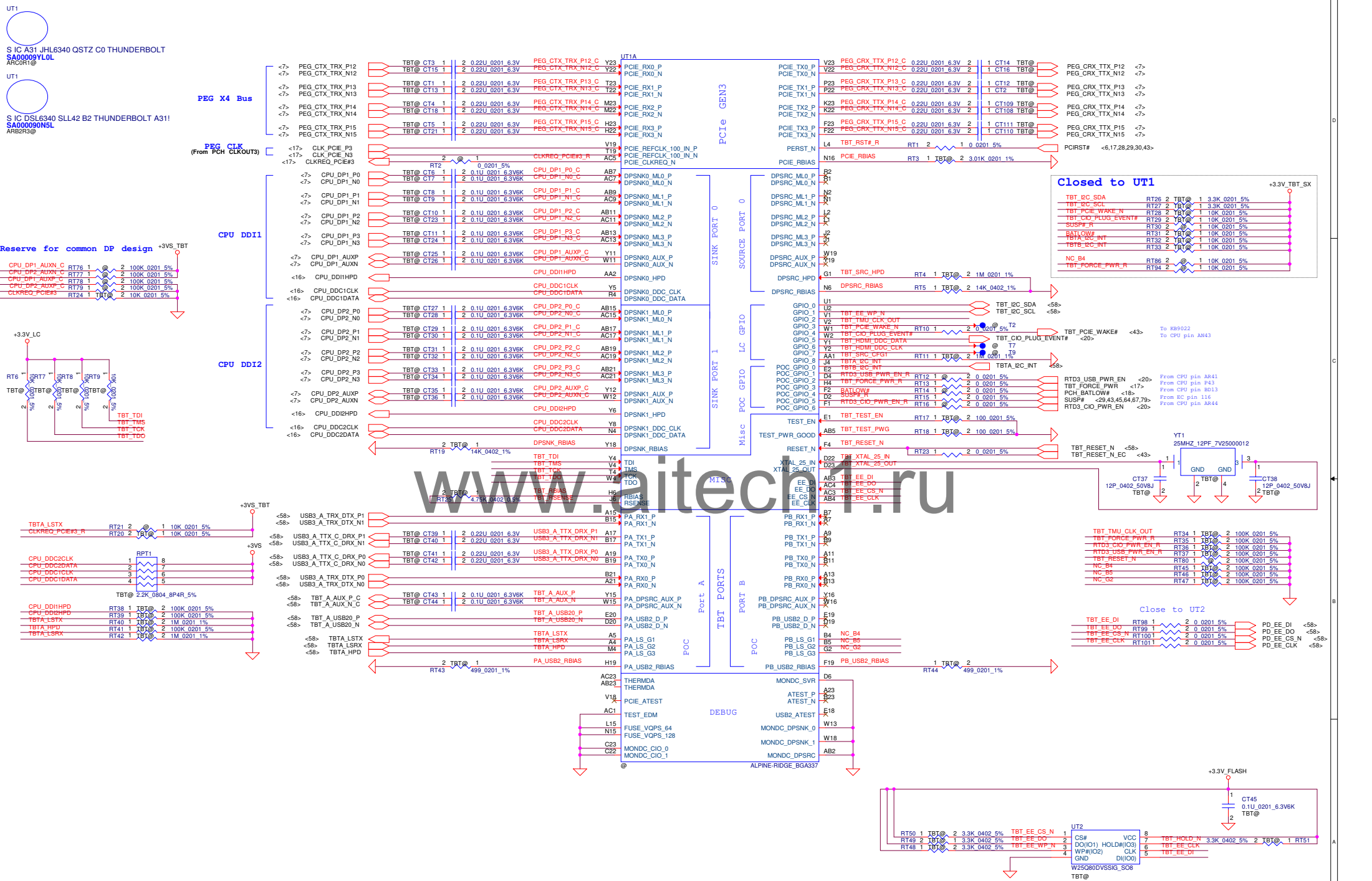


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Date:	January 05, 2016	Sheet	53	of 82
		Rev	0.2	



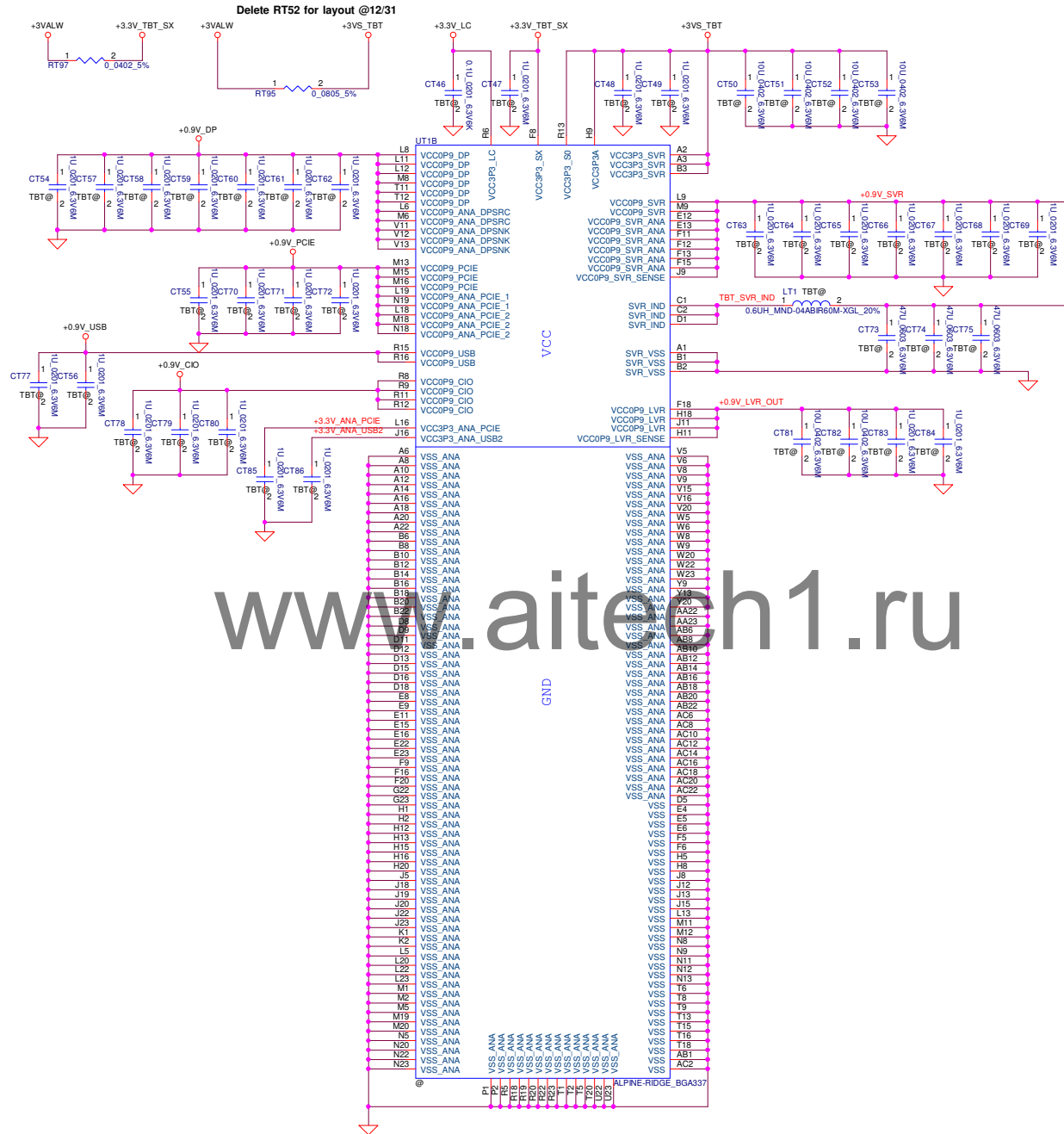
	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	2	3		12	





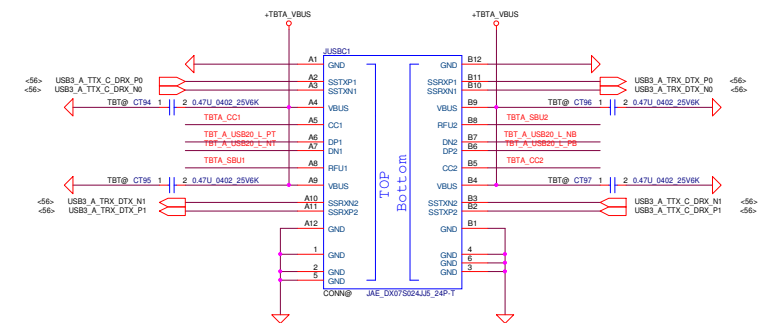
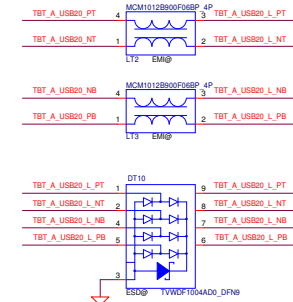
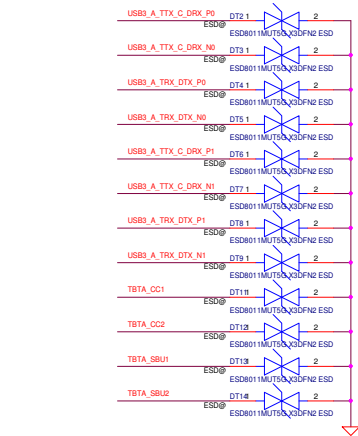
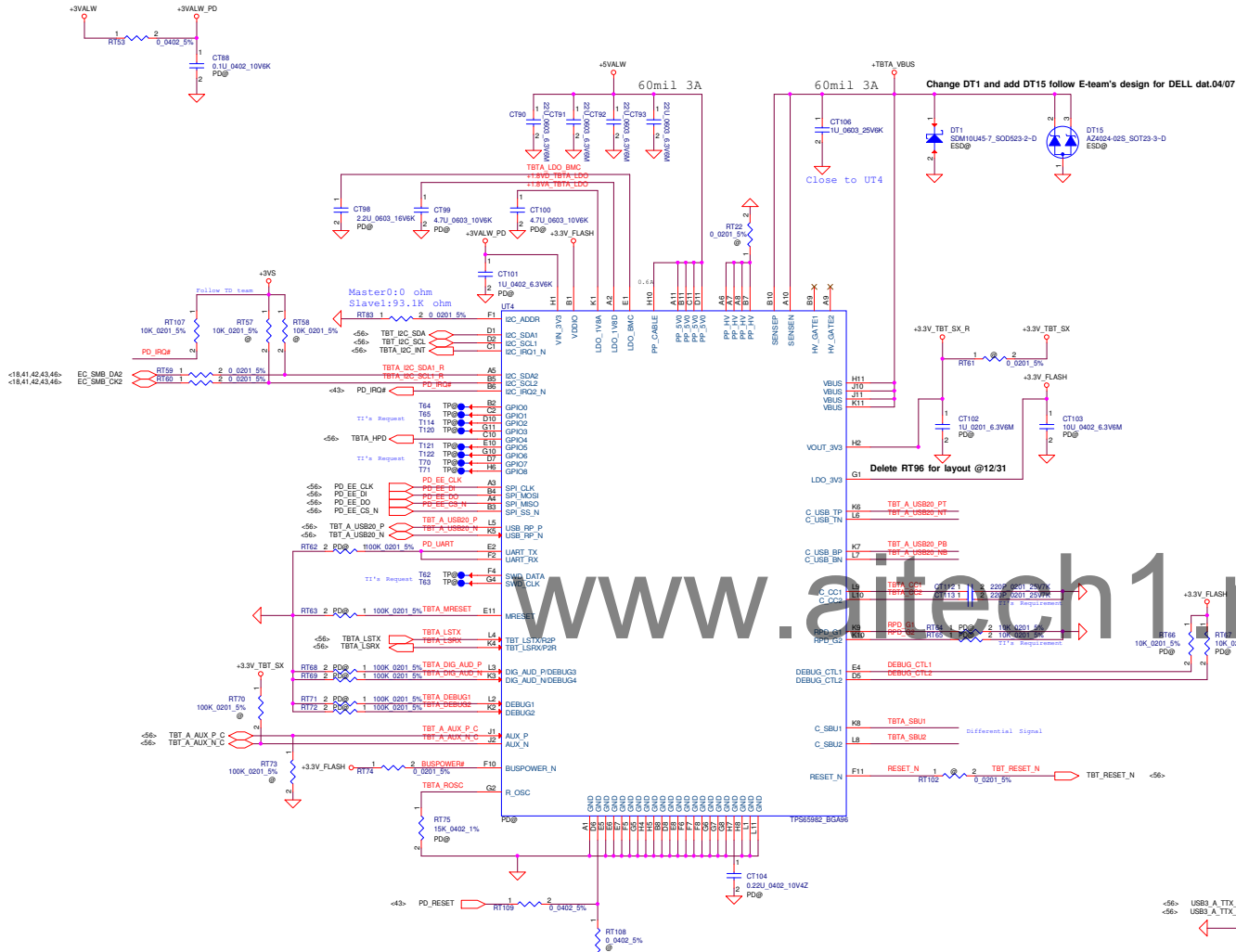
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2016/01/06		Title	
		Deciphered Date		Thunderbolt (1/2)	
		2017/01/06		Size	
				Document Number	
				LA-D753P	
				Date:	
				Tuesday, July 05, 2016	
				Sheet	
				56 of 82	

Delete RT104 for layout @12/31

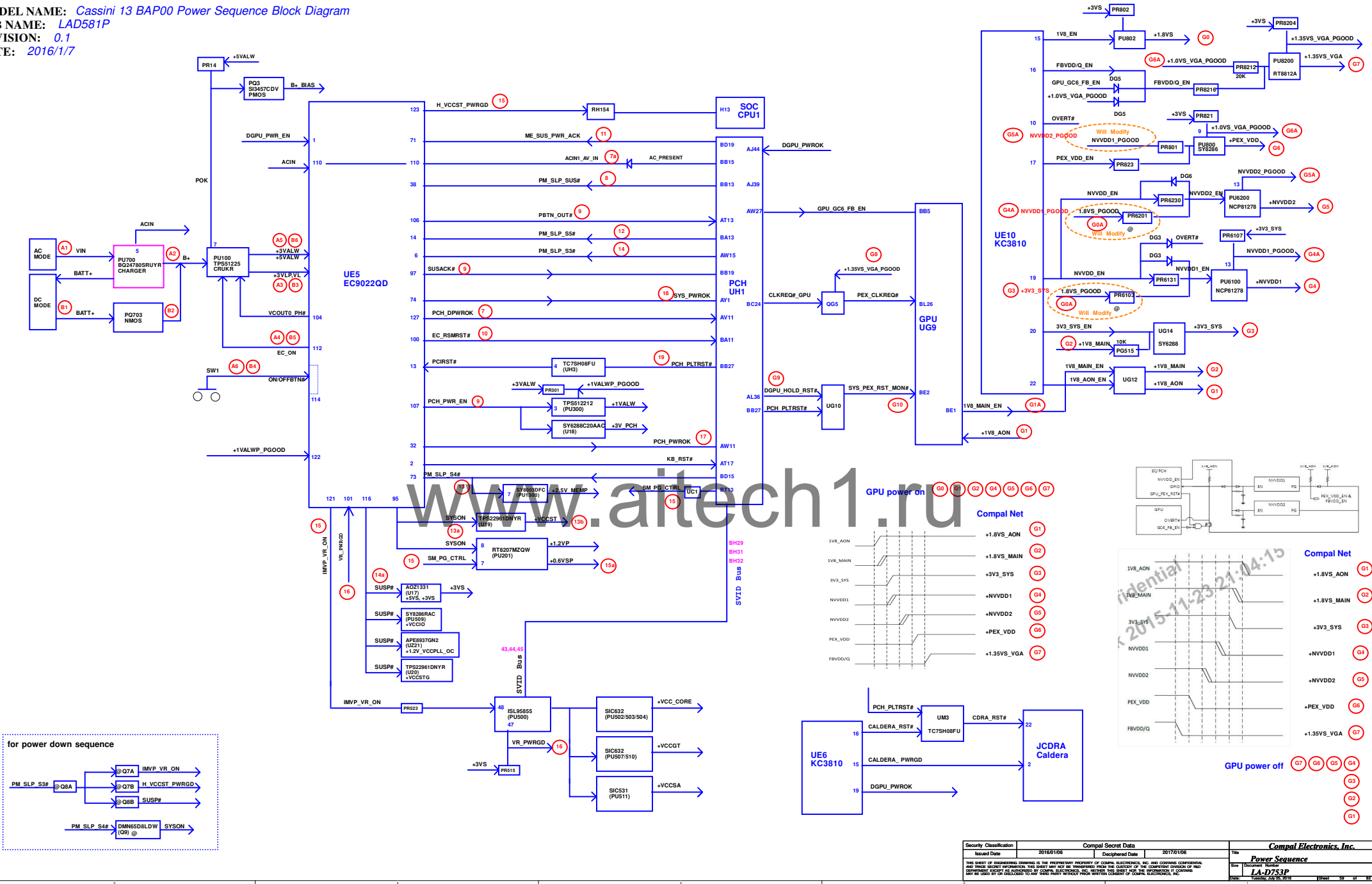


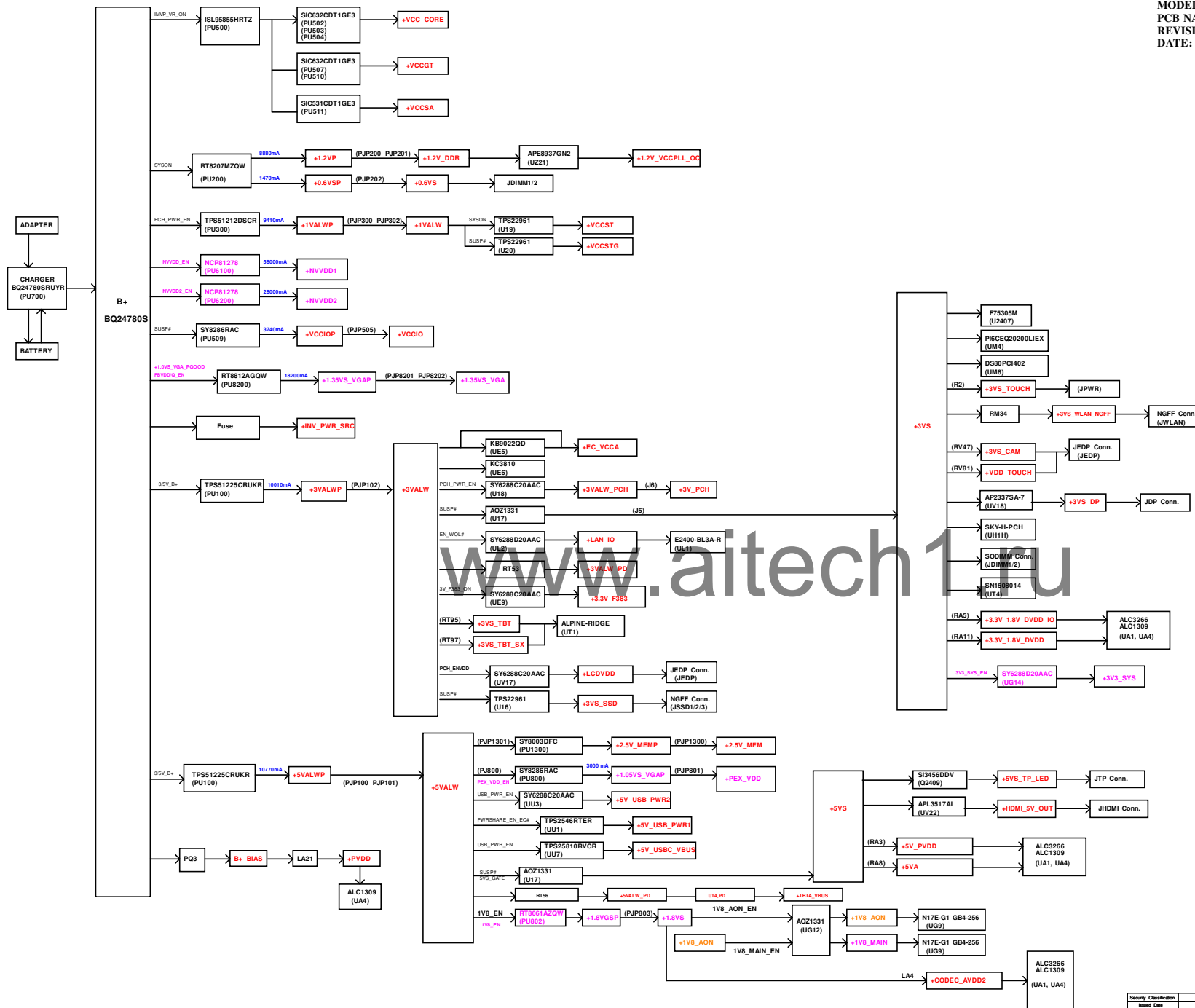
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	Thunderbolt (2/2)
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				Date:	Tuesday, July 05, 2016
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				LA-D753P	













CC = 7168mA  
CV = 17.7V

I<sub>ada</sub>=0~12.3A(240W)  
I<sub>ada</sub>=0~16.92A(330W)

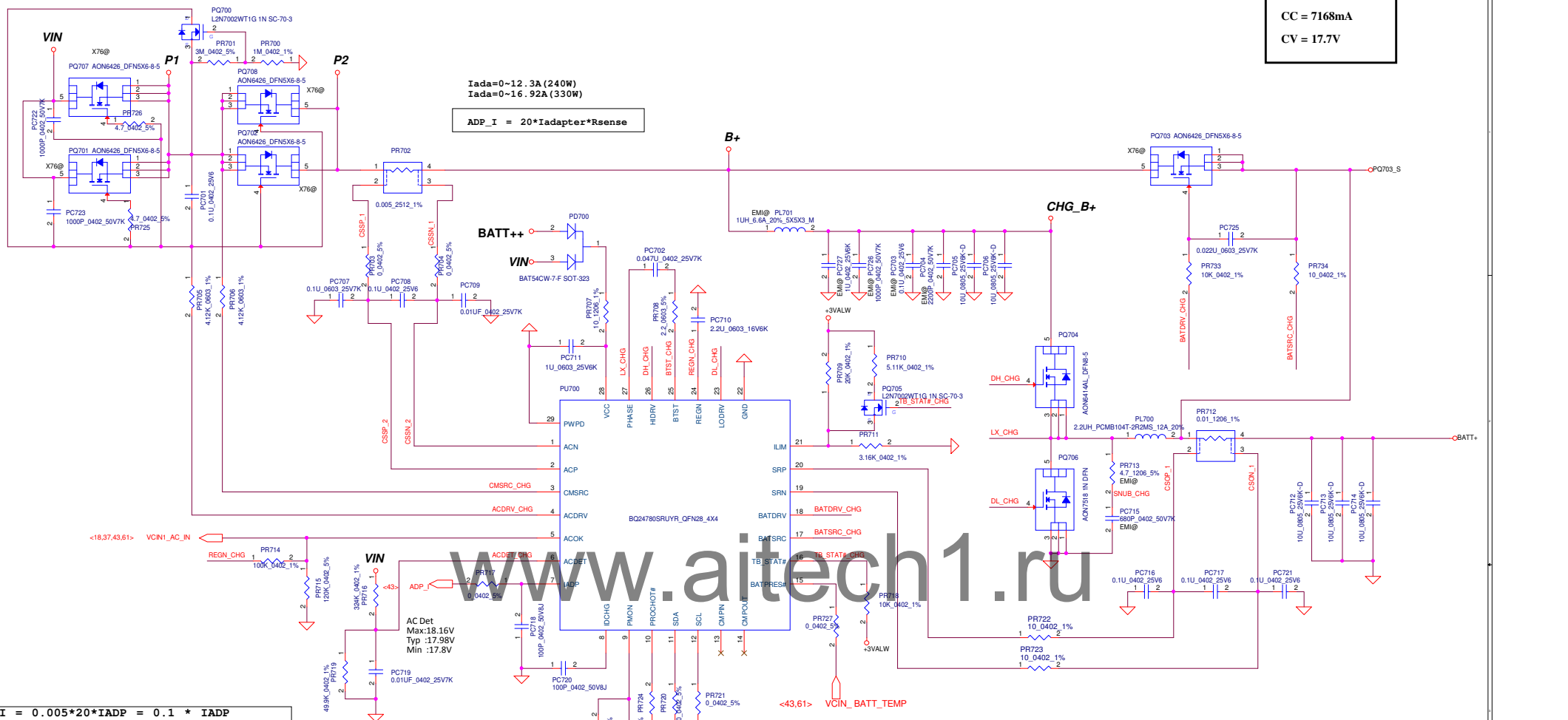
ADP\_I = 20\*I<sub>adapter</sub>\*R<sub>sense</sub>

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ADPI = 0.005\*20\*IADP = 0.1 \* IADP

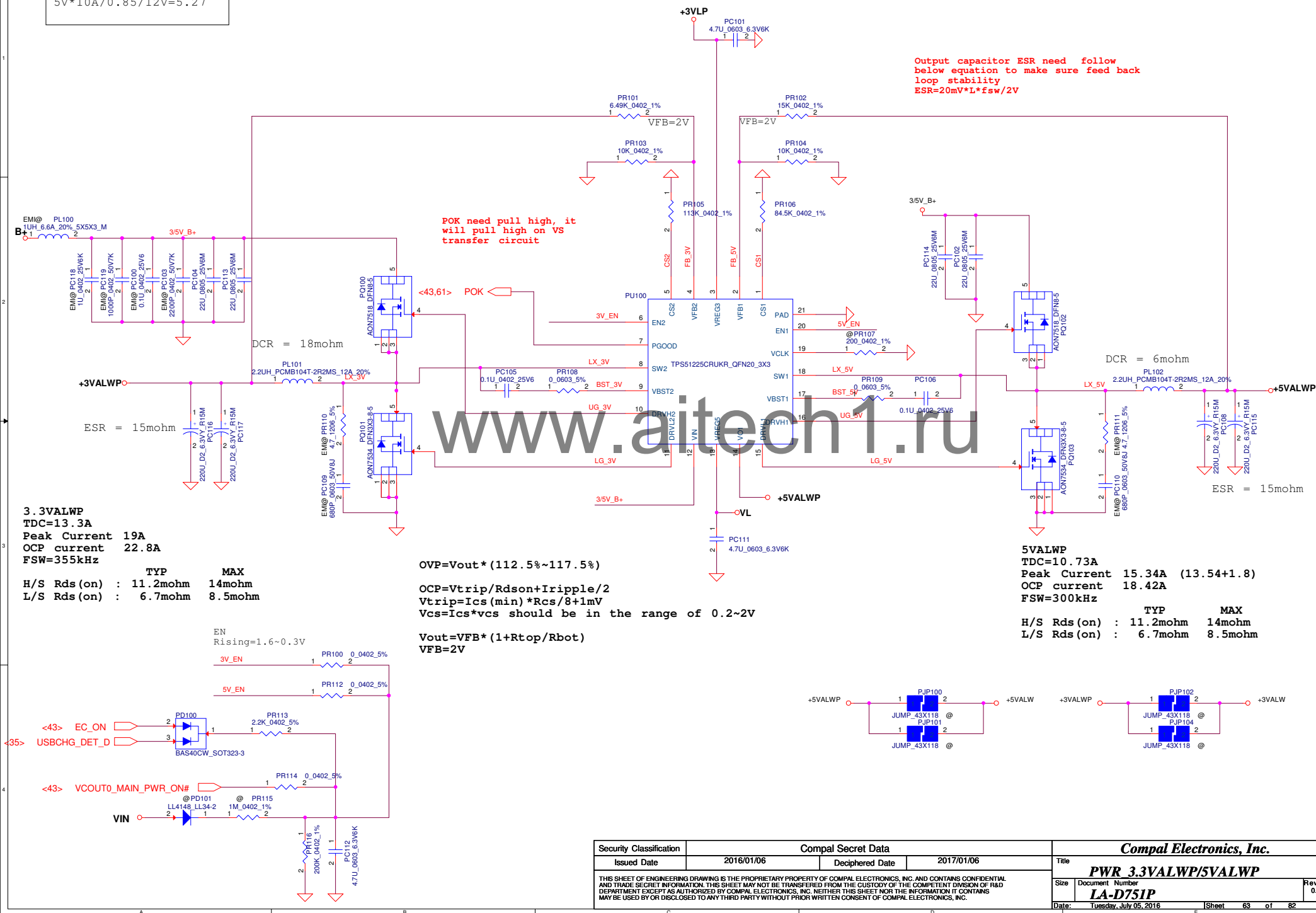
Adapter = 240W  
CP = 240W/19.5V\*0.9 = 11.07A  
ADPI = 1.11V  
Hybrid trigger = CP\*107% = 11.85A  
ADPI = 1.19V  
IPCC = 240W/19.5V\*0.95 = 11.69A  
ADPI = 1.17V  
IPCC(hybrid mode) = 240W/19.5V = 12.31A  
ADPI = 1.23V  
PROCHOT = 240W/19.5V+1 = 13.3A  
ADPI = 1.33V

Adapter = 330W  
CP = 330W/19.5V\*0.9 = 15.23 A  
ADPI = 1.52V  
Hybrid trigger = CP\*107% = 16.3A  
ADPI = 1.63V  
IPCC = 330W/19.5V\*(1+0.95) = 16.08A  
ADPI = 1.61V  
IPCC(hybrid mode) = 330W/19.5V = 16.92A  
ADPI = 1.69V  
PROCHOT = 330W/19.5V+1 = 17.92A  
ADPI = 1.79V



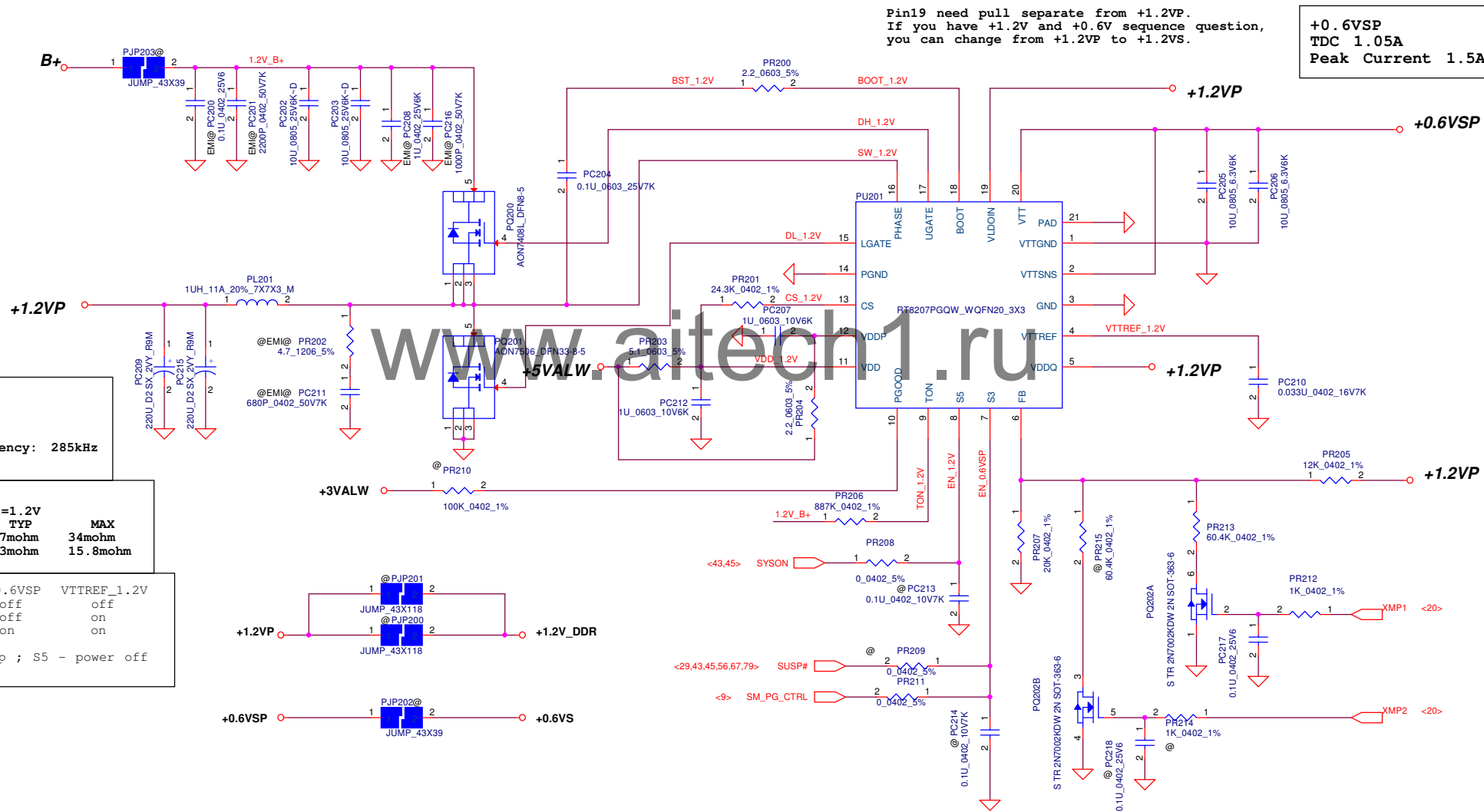
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR CHARGER
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				Date: Tuesday, July 05, 2016	Sheet 82 of 82

Input Current: 7.5A  
 $3.3V \cdot 10A / 0.85 / 12V = 2.23$   
 $5V \cdot 10A / 0.85 / 12V = 5.27$



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Input Current: 1A  
 $1.2V \cdot 8.88A / 0.85 / 12V = 1$



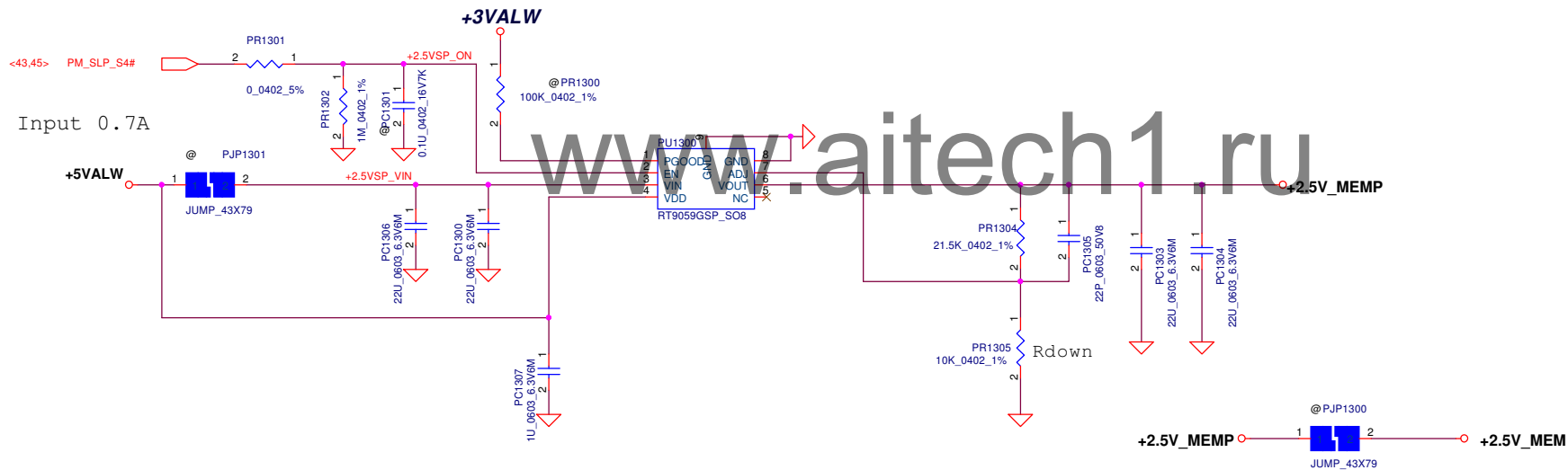
+1.2VP  
TDC=9A  
Ipeak=12.86A  
OCP=15.43A  
Switching Frequency: 285kHz

OVP: 110%~120%	
VFB=0.75V, Vout=1.2V	
	TYP MAX
H/S Rds (on) :	27mohm 34mohm
L/S Rds (on) :	13mohm 15.8mohm

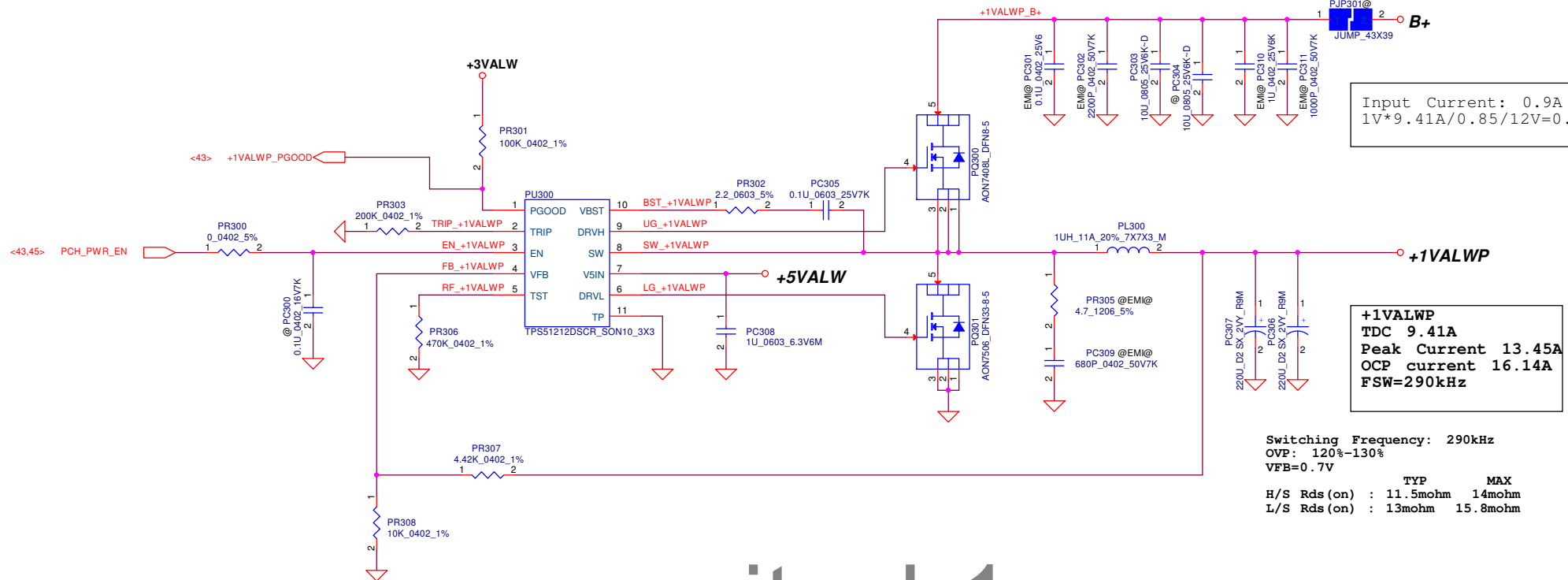
Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

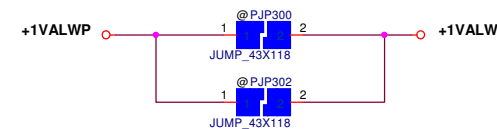
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				Size	Document Number	Rev
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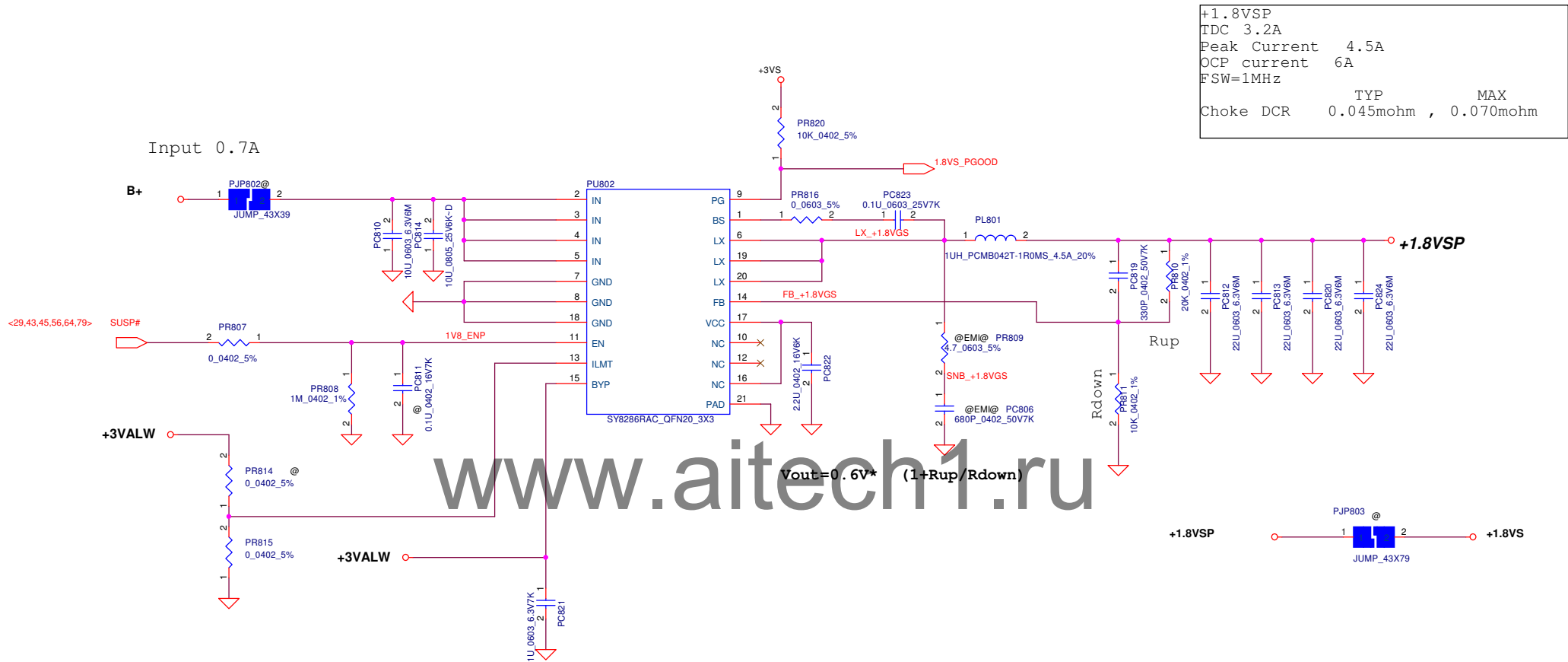
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR +2.5V MEM
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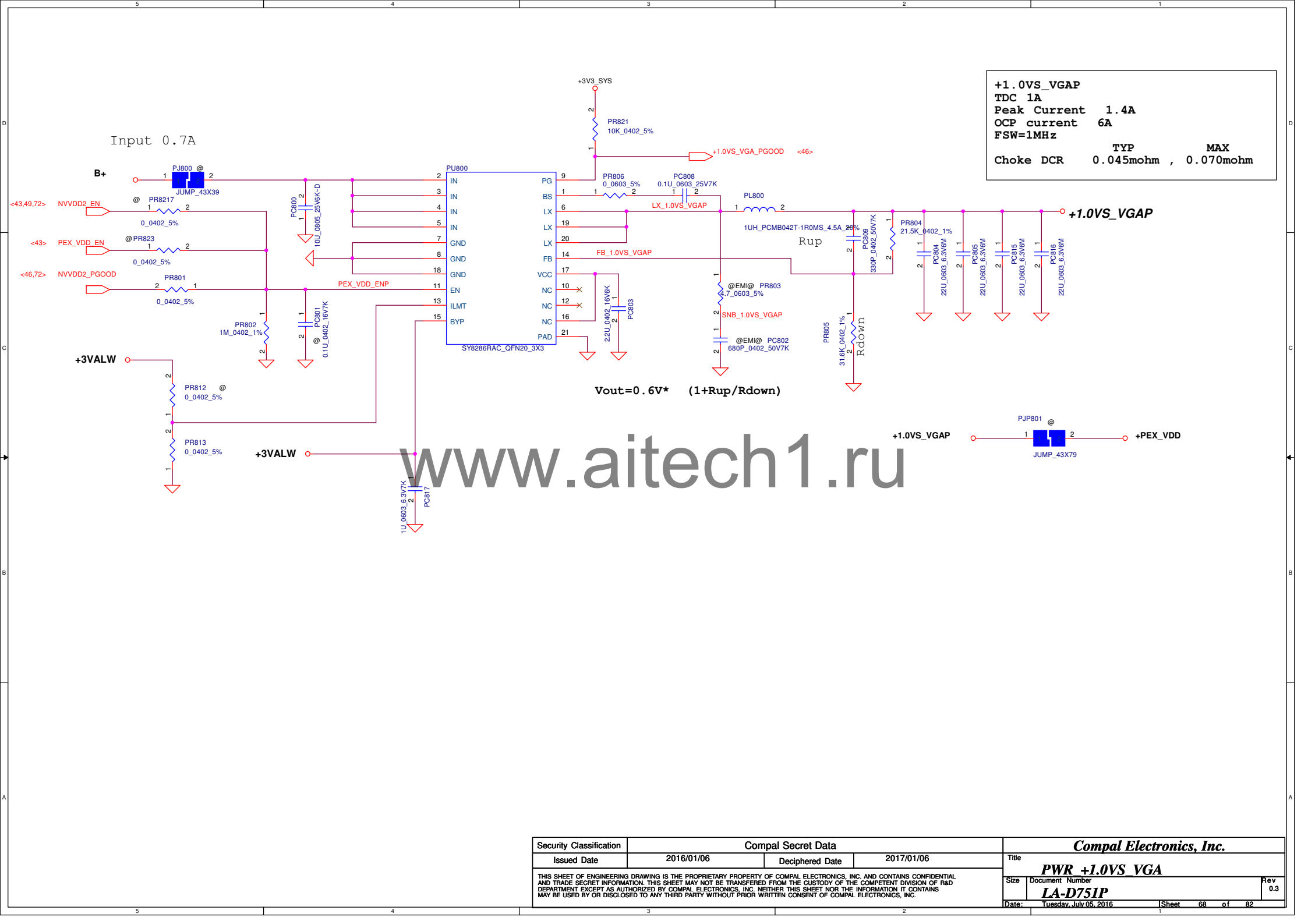
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				PWR +1VALWP				
				Size		Document Number		Rev
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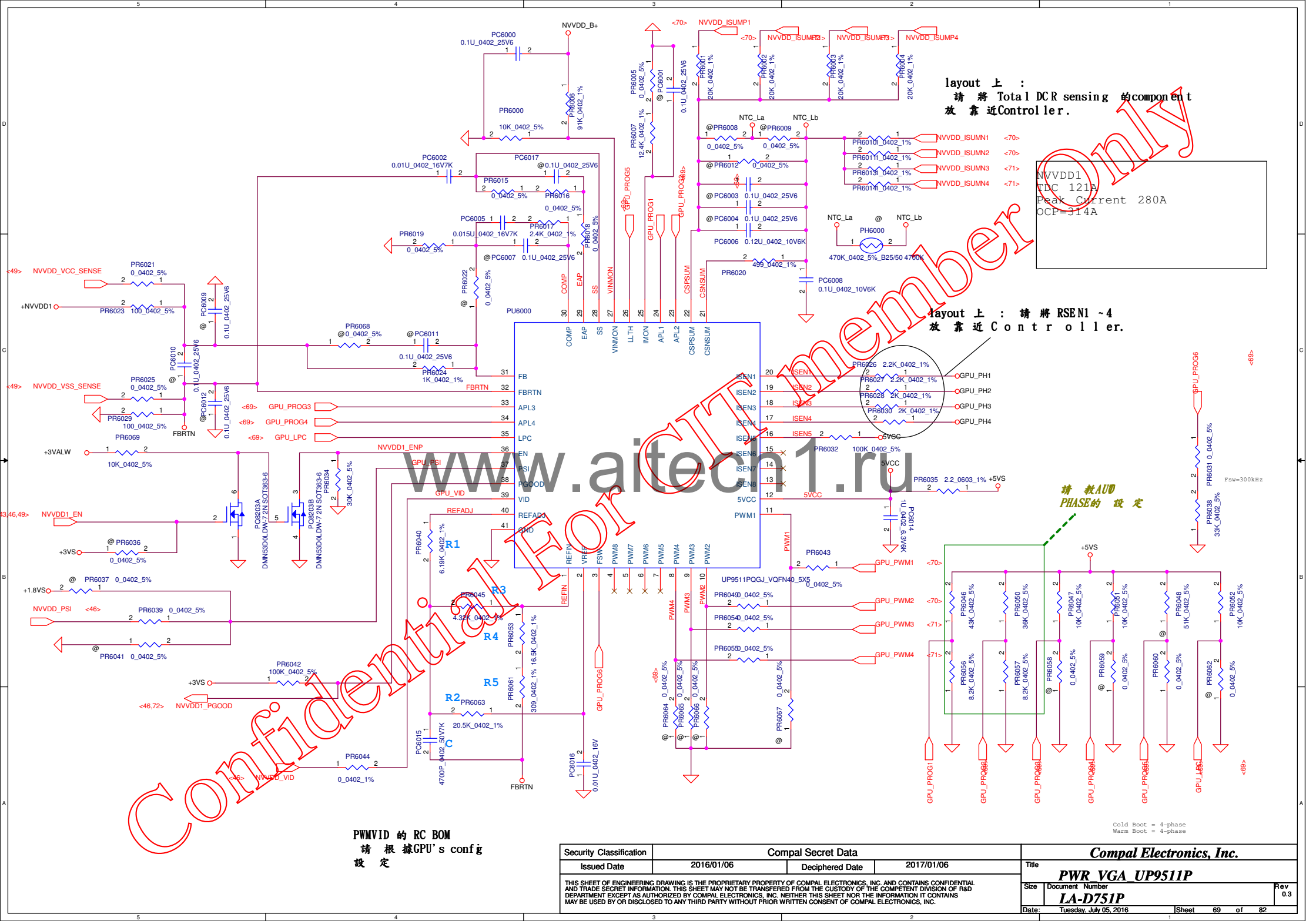
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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**+1.0VS\_VGAP**  
TDC 1A  
Peak Current 1.4A  
OCP current 6A  
FSW=1MHz  
Choke DCR 0.045mohm , 0.070mohm  
TYP MAX

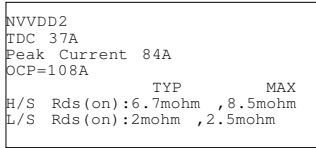
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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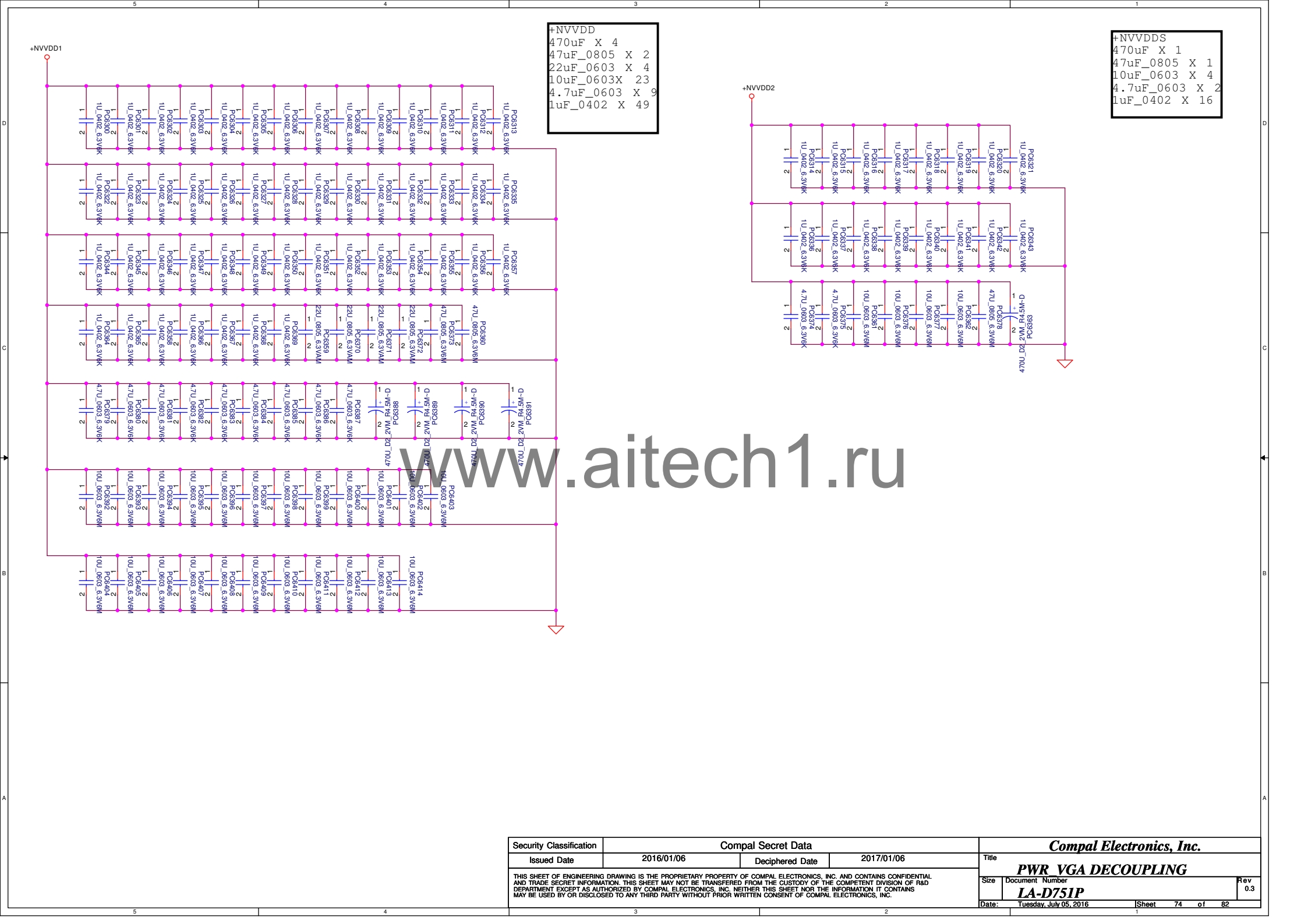






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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	<b>PWR +NVVDD2</b>	
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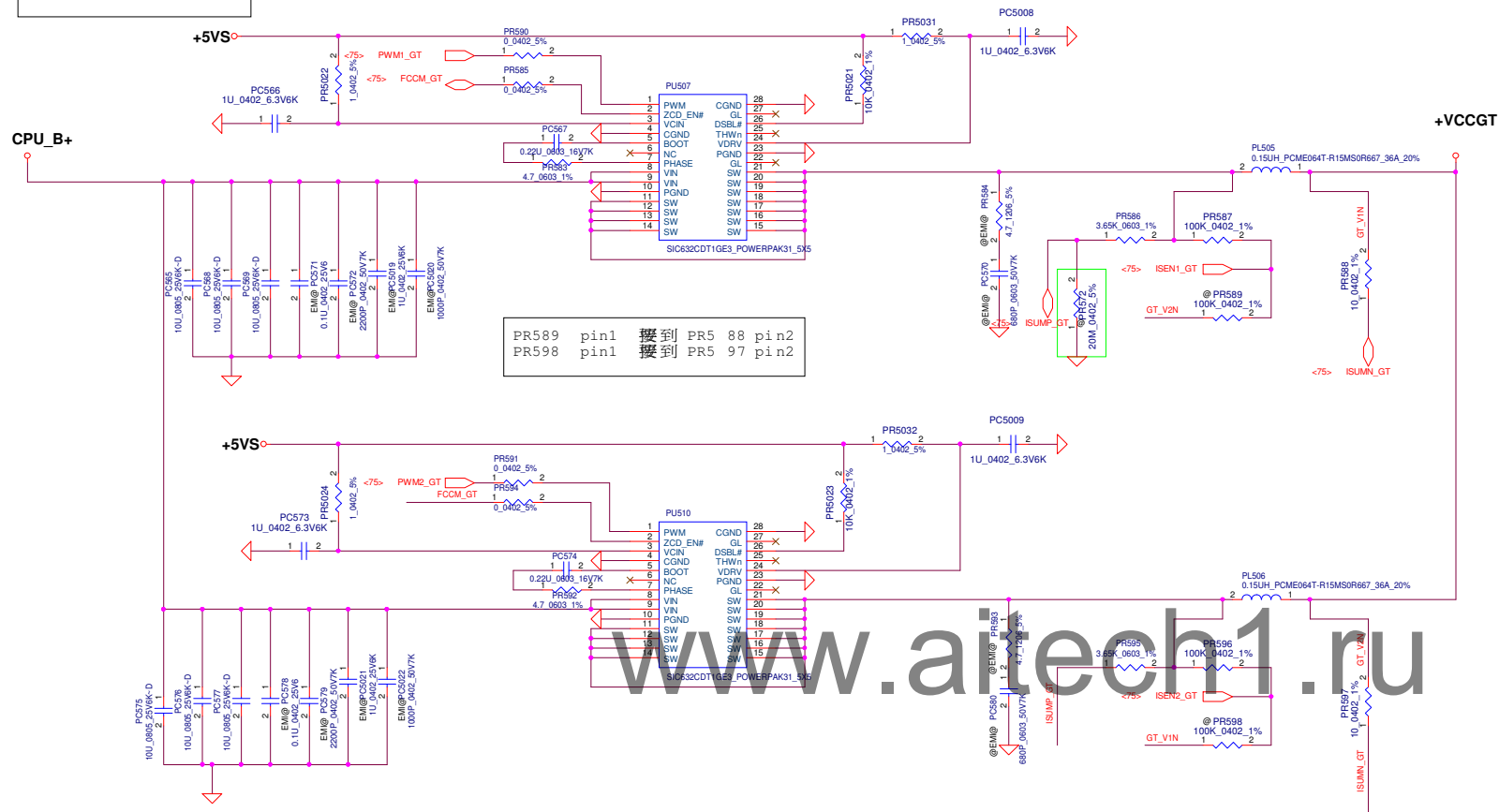
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
				PWR VGA DECOUPLING	
				Size	Document Number
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Input Current: 5.7A  
1.5V\*39A/0.85/12V=5.7

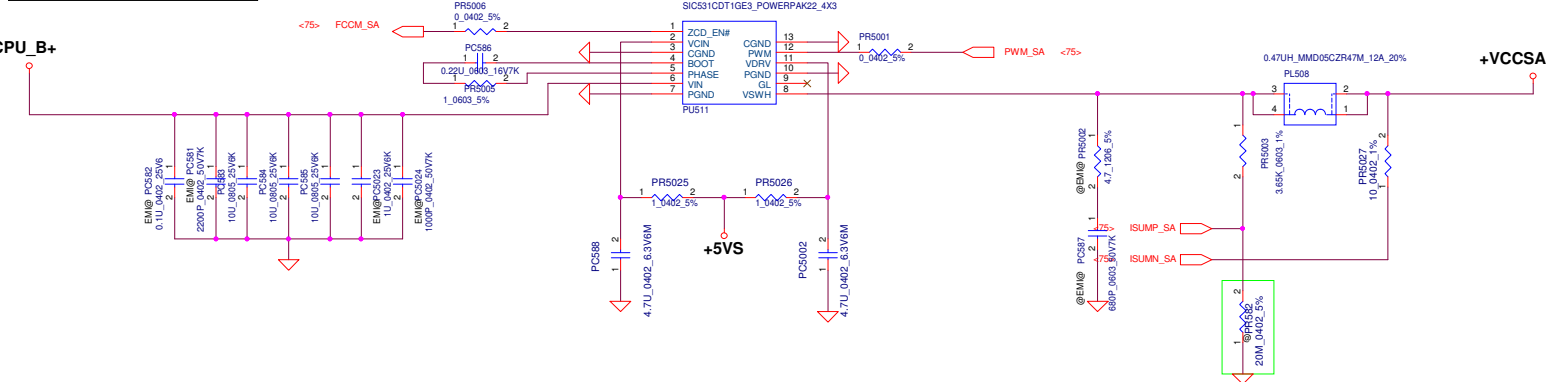


PR589 pin1 接到 PR5 88 pin2  
PR598 pin1 接到 PR5 97 pin2

+VCC\_GT  
TDC PL2 :39A  
Peak Current 54A  
OCP Current 64.8A  
DCR 0.66mohm +/-7%  
Load Line 2.65mV/A

+VCC\_SA  
TDC PL2 :10A  
Peak Current 11A  
OCP Current 13.2A  
DCR 7.4mohm typ  
Load Line 9.1mV/A

Input Current: 1.0A  
1.05V\*10A/0.85/12V=1.0



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+VCC\_CORE

+VCCGT

+VCCSA

VCC\_CORE  
220uF X3  
47uF\_0805 X 4  
22uF\_0603 X 8  
10uF\_0402 X 28  
1uF\_0201 X 63

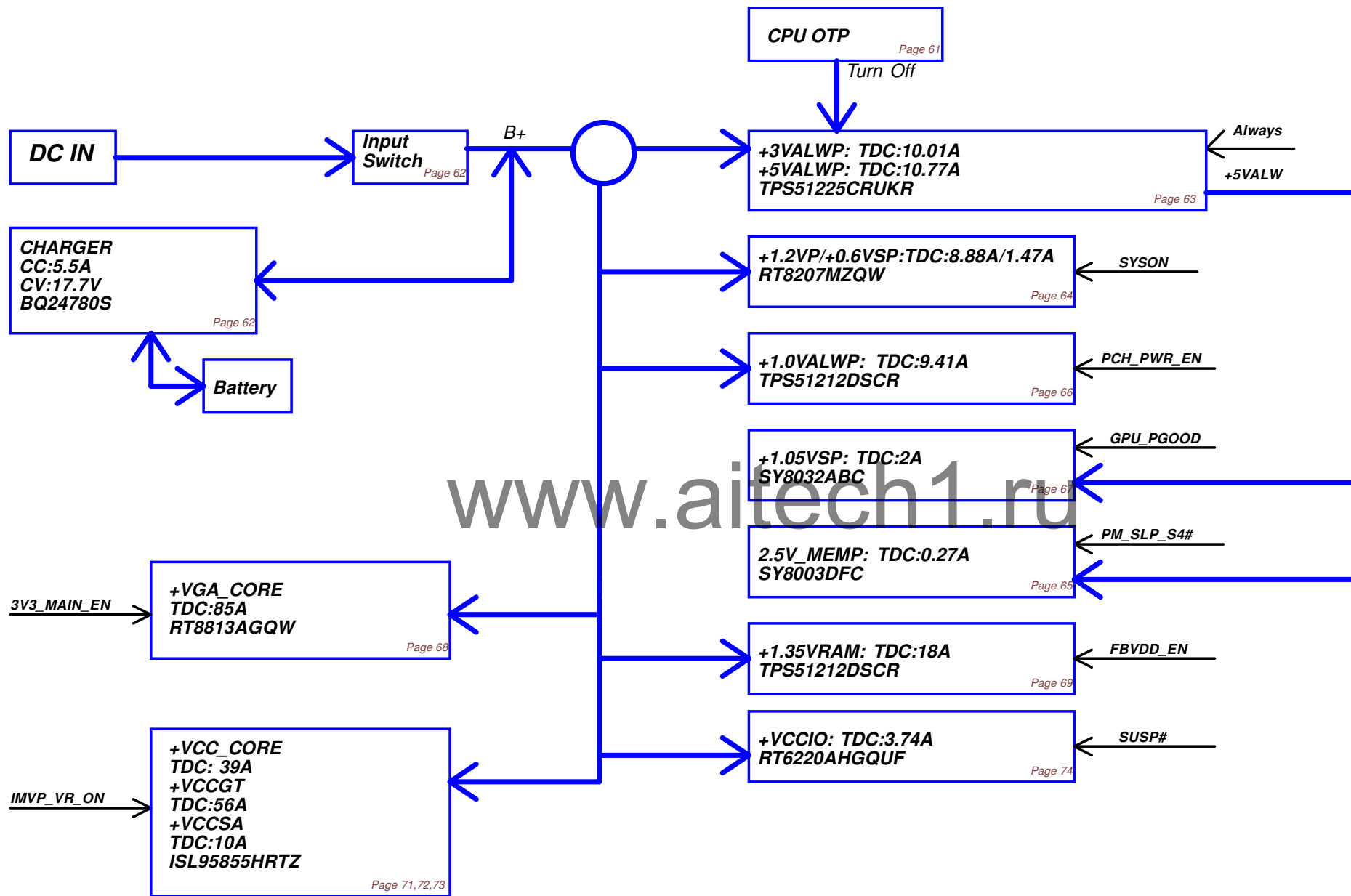
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47uF\_0805 X 6  
22uF\_0603 X 8  
10uF\_0402 X 3  
1uF\_0201 X 68

VCC\_SA  
220uF X1  
47uF\_0805 X 1  
10uF\_0402 X 7  
1uF\_0201 X 3

Security Classification		Compal Secret Data		Title	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	PWR-CPU DECOUPLING	
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# Power block



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR POWER BLOCK DIAGRAM
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## Version Change List ( P. I. R. List ) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	69	VGA_UP9511P	2016/03/28	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6020 from 100 Ohm to 500 Ohm. 2. Change PR6007 from 5.1k Ohm to 13.3k Ohm	0.2
2	64	+1.2VP/+0.6VSP	2016/03/28	Compal_PWR	Add component for XMP	1. Change PR213 from 20k Ohm to 60.4k Ohm.	0.2
3	69	VGA_UP9511P	2016/03/30	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6069&PR6036 pin 1 from +3V3_SYS to +3VALW .	0.2
4	69	VGA_UP9511P	2016/04/01	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6033 connect to NVVDD_EN.	0.2
5	72	+NVVDD2	2016/04/01	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6402 connect to NVVDD_EN.	0.2
6	73	+1.35VS_VGAP	2016/04/11	Compal_PWR	For NV request.	1. Change +3VS to +1.8V_AON	0.2
7	64	+1.2VP/+0.6VSP	2016/04/11	Compal_PWR	Add component for XMP	1. Add PR212 to 1k Ohm. 2. Add PC217 to 0.1uF. 3. Add PQ202 MOS.	0.2
8	73	+1.35VS_VGAP	2016/04/11	Compal_PWR	For BOM control	1. Add PR8211 of 34.8k Ohm for SAMSUNG@ 2. Add PR8211 of 30k Ohm for MIRCON@ 3. Add PR8215 of 52.3k Ohm for SAMSUNG@ 4. Add PR8215 of 68.1k Ohm for MIRCON@ .	0.2
9	68	+1VS_VGAP	2016/04/11	Compal_PWR	For +1VS_VGAP OCP setting.	1. Change PL800 from 1UH_MAMK2520T1R0M_3.1A to 1UH_PCMB042T-1R0MS_4.5A.	0.2

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				Size	Document Number	Rev
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	75	VCORE_ISL95829	2016/05/18	Compal_PWR	For CPU_VCORE setting.	1. Change PC507 from 680pF to 1000pF. 2. Change PC517 from 0.047uF to 0.068uF. 3. Change PR548 from 95.3kohm to 105kohm.	0.3
11	62	CHARGER	2016/05/18	Compal_PWR	For CHARGER ILIM setting.	1. Change PR710 from 2kohm to 5.11kohm. 2. Change PR711 from 2.43kohm to 3.16kohm.	0.3
12	68	+1.0VS_VGAP	2016/05/18	Compal_PWR	Add component for +1.0VS_VGAP_EN	1. Add PR801 for 0ohm.	0.3
13	69	VGA_UP9511P	2016/05/18	Compal_PWR	For VGA_UP9511P_EN	1. Change PQ8203 from TR DMN66D0LDW-7 2N SOT363-6 to TR DMN53D0LDW-7 2N SOT363-6.	0.3
14	73	+1.55VRAM	2016/06/20	Compal_PWR	Add component for +1.55VRAM	1. Add PR8219 or 0ohm.	0.4
15	62	CHARGER	2016/06/20	Compal_PWR	For charger setting.	1. Add PQ701, PQ702, PQ707, PQ708, PQ703 of AON7506_DFN33-8-5 for X760	0.4

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				Size	Document Number	Rev
					LA-D751P	0.3
				Date:	Tuesday, July 05, 2016	Sheet 82 of 82